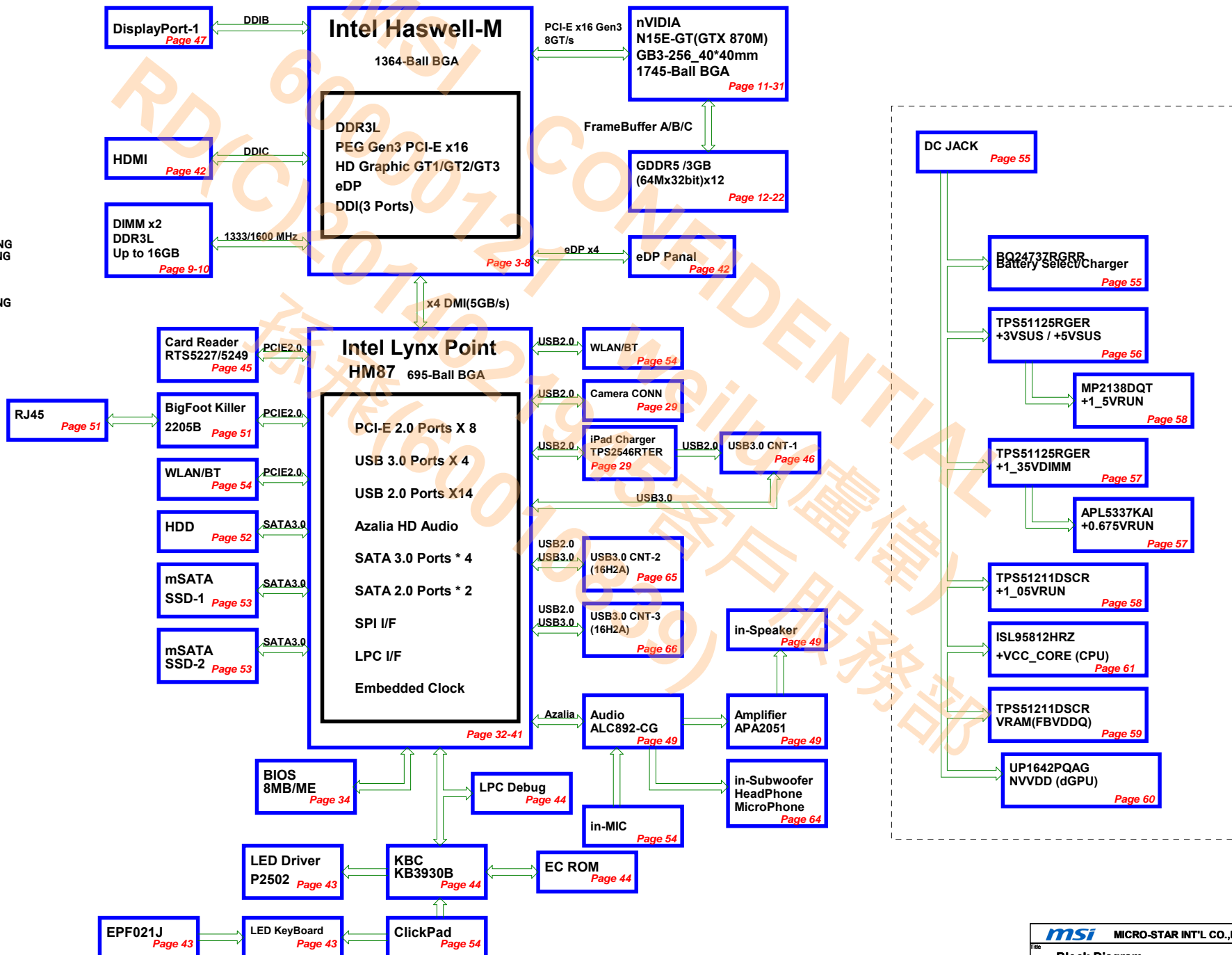


Page 01:	Block Diagram
Page 02:	Platform
Page 03:	CPU-1 (Host Bus)
Page 04:	CPU-2 (DDR3L)
Page 05:	CPU-3 (Display/Reserved)
Page 06:	CPU-4 (Power)
Page 07:	CPU-6 (Power & GND)
Page 08:	CPU-5 (GND)
Page 09:	DDR3L SODIMM 0
Page 10:	DDR3L SODIMM 1
Page 11:	DGPU PCI-E Host
Page 12:	DGPU_MEM IF A/B
Page 13:	DGPU_GDDR5 FrameBuffer A0
Page 14:	DGPU_GDDR5 FrameBuffer A1
Page 15:	DGPU_GDDR5 FrameBuffer B0
Page 16:	DGPU_GDDR5 FrameBuffer B1
Page 17:	DGPU_GDDR5 FB-A_DECOUPLING
Page 18:	DGPU_GDDR5 FB-B_DECOUPLING
Page 19:	DGPU_MEM IF C/D
Page 20:	DGPU_GDDR5 FrameBuffer C
Page 21:	DGPU_GDDR5 FrameBuffer C
Page 22:	DGPU_GDDR5 FB-C_DECOUPLING
Page 23:	DGPU_GPU DECOUPLING A
Page 24:	DGPU_GPU DECOUPLING B
Page 25:	DGPU_DACA_Display IF
Page 26:	DGPU_GPIO_I2C
Page 27:	DGPU_MIO & XTAL
Page 28:	DGPU_ROM_HW Straps
Page 29:	DGPU_NVDD, FBVDDQ
Page 30:	DGPU_GND
Page 31:	DGPU_Power Control
Page 32:	PCH-1 (HDA/JTAG/SATA)
Page 33:	PCH-2 (CLK)
Page 34:	PCH-3 (LPC, SMBUS)
Page 35:	PCH-4 (DMI, FDI)
Page 36:	PCH-5 (PCI, DDI)
Page 37:	PCH-6 (GPIO, MISC)
Page 38:	PCH-7 (PCI, USB)
Page 39:	PCH-8 (Power)
Page 40:	PCH-8 (Power)
Page 41:	PCH-8 (GND)
Page 42:	eDP Connector
Page 43:	LED Driver IC/LED_8051
Page 44:	KBC( KB3930QFB1 )
Page 45:	Card Reader/USB3.0 CNT-1/-2
Page 46:	USB 3.0 / iCharger
Page 47:	DP with Repeater
Page 48:	HDMI Repeater
Page 49:	Audio CODEC/Audio AMP
Page 50:	CPU FAN/BTB CONN
Page 51:	GIGA LAN(BigFoot BFN2205B)
Page 52:	HDD With Repeater
Page 53:	SSD/ DGPU FAN
Page 54:	WLAN / Camera/ClickPad/LID
Page 55:	Battery Select/Charger
Page 56:	System Power
Page 57:	+1.35VDIMM/+0.675VRUN
Page 58:	+1.05VRUN / +1.5VRUN
Page 59:	DGPU POWER FBVDDQ
Page 60:	DGPU POWER NVDD
Page 61:	CPU Power (ISL95812HRZ)
Page 62:	EMI
Page 63:	Screw/ME
Page 64:	[A] Audio
Page 65:	[A] USB3.0 CNT-3/-4
Page 66:	LED Board
Page 67:	Power SW Board
Page 68:	Power Delivery Map
Page 69:	Power on Block Diagram
Page 70:	Power down Sequence
Page 71:	Power on Sequence



SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

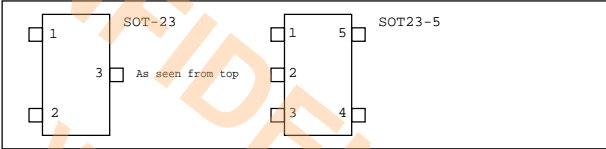
Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_35VDIMM	1.35V DDR3L power rail (off in S4-S5)	PM_SLP_S5#
+0_675VRUN	0.675V DDR3L Termination voltage (off in S3-S5)	PM_SLP_S3#
+5VRUN	5.0V switched power rail (off in S3-S5)	RUN_ON
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUN_ON
+1_5VRUN	1.5V switched power rail (off in S3-S5)	PM_SLP_S3#
+VCC_CORE	1.8V Core Voltage for Processor	EC_ALLSYSPPG
+1_05VRUN	1.05V rail for Processor	PM_SLP_S3#
NVVD	V Core Voltage for nVIDIA dGPU	NVVD_EN
+3V3_NV	3.3V PEX power rail (off in Optimus OFF)	DGPU_PWR_EN#
FBVDDQ	1.35V FB / GDDR5 power rail (off in Optimus OFF)	FBVDDQ_ON
PEX_VDD	1.05V PLL power rail (off in Optimus OFF)	NVVD_EN

Net Naming Conventions

<b>Suffix</b>
# = Active Low Signal
<b>Prefix</b>
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)
FB = DGPU VRAM
VIAxxx = Like Test Point, but using VIA.

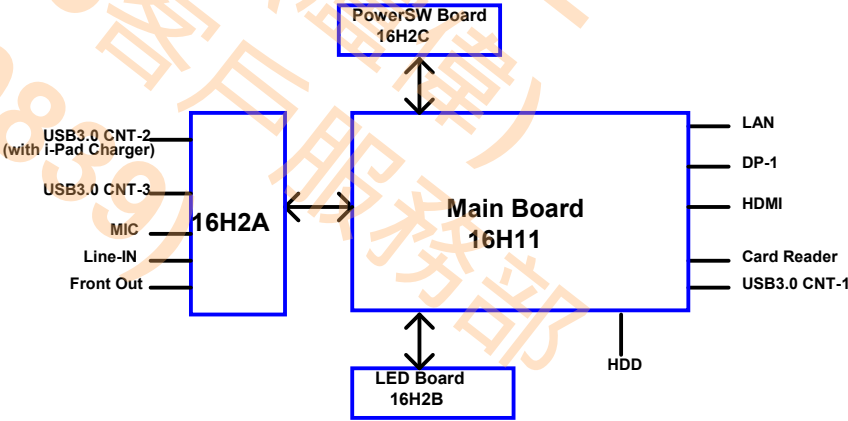
PCB Footprints



POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+*VSUS	+*VRUN	Clocks
S0( Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3( Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4( Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on and +V\*SUS always keep high



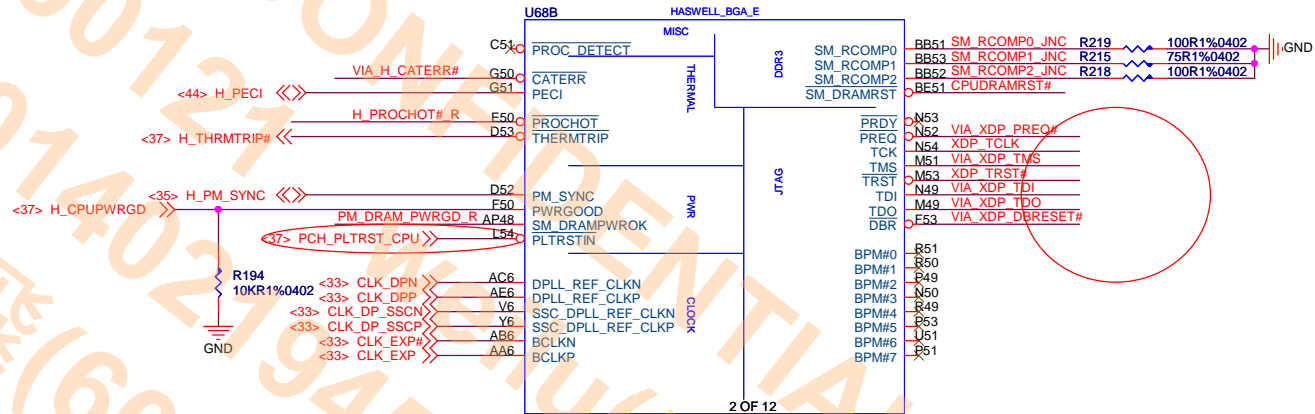
# Haswell ( DMI,PEG,FDI )

PEG\_RCOMP  
Width:12 mils  
Spacing:15 mils  
Length:400 mils

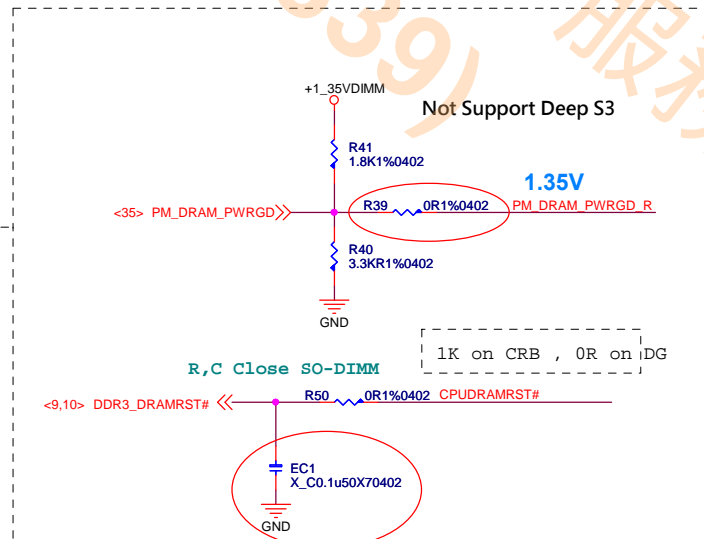


# Haswell ( CLK,MISC,JTAG )

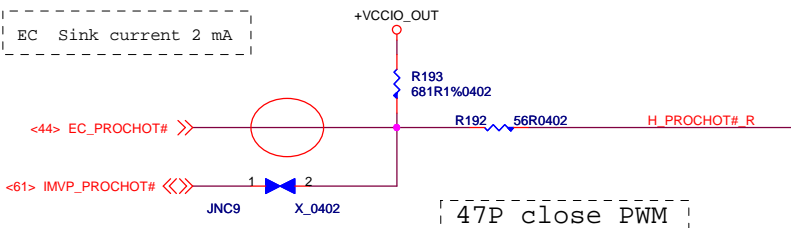
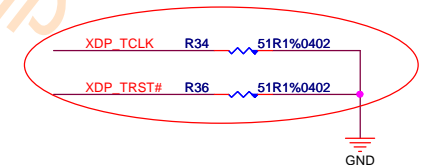
SM\_RCOMP\_0/1/2 : 15/20/25/15/20/25  
SM\_RCOMP\_0/1/2 Length max: 500mil



H\_CUPUPWRGD EC8 X C15p50N0402 GND



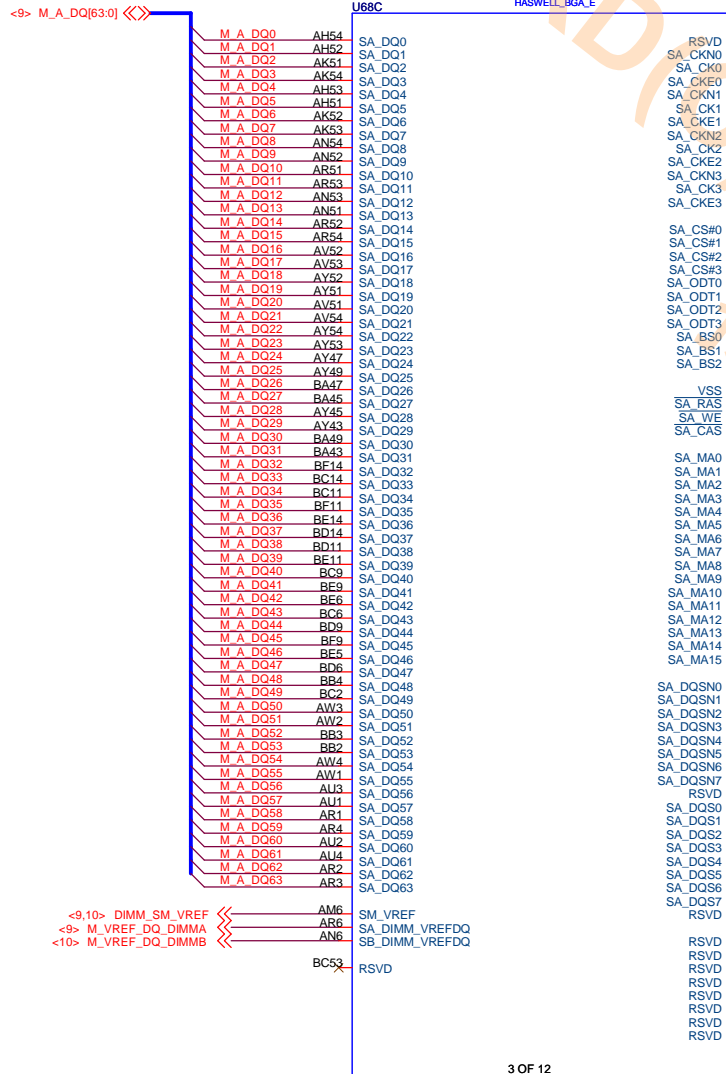
p.11 479493\_479493\_SharkBay\_HSW\_ext\_rev2.0.pdf  
Processor JTAG (TDI, TDO, TMS, TRST#, TCK) signals, PREQ# and PRDY# signals have adequate internal bias resistances to support the removal of the external pull up and pull down on the board when debug is no longer needed.



# Haswell ( DDR3L )

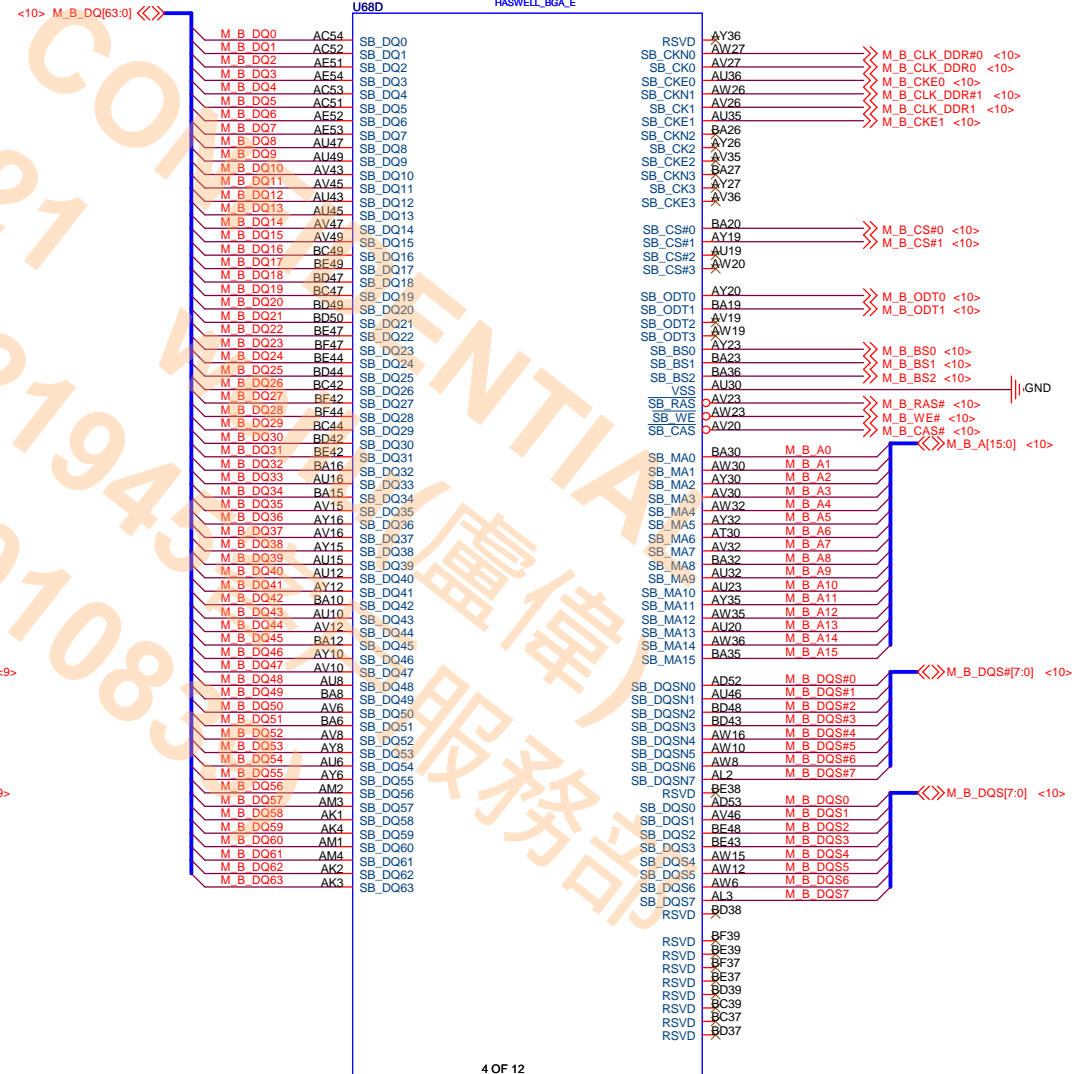
## SODIMM#A

HASWELL\_BGA\_E



## SODIMM#B

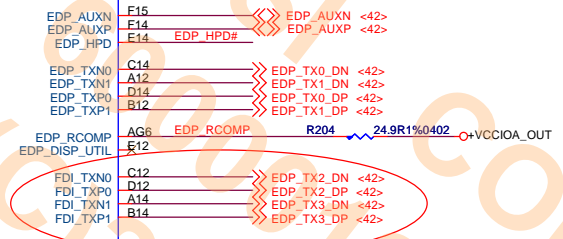
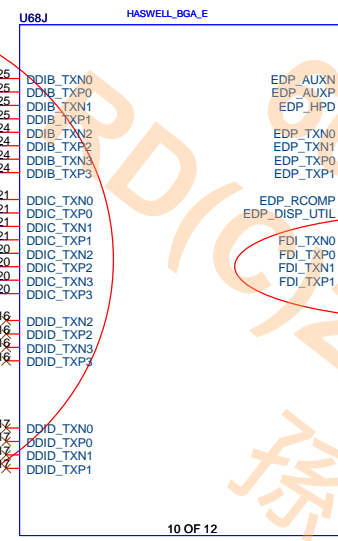
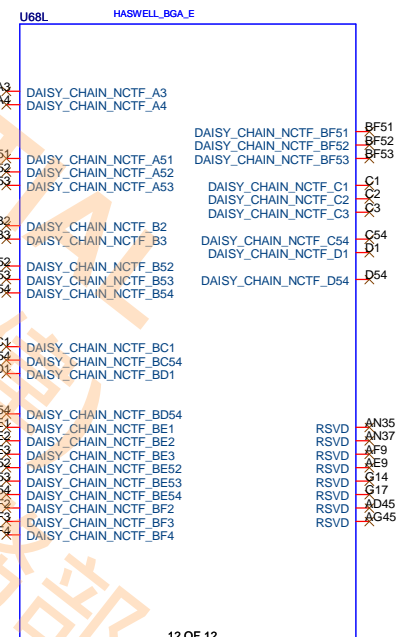
HASWELL\_BGA\_E



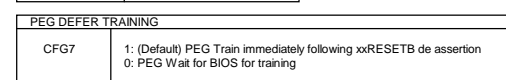
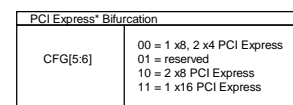
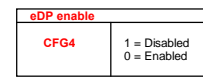
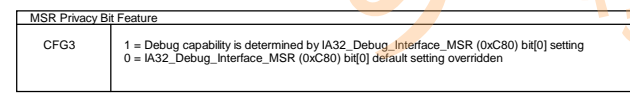
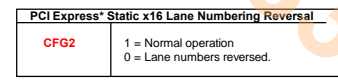
The diagram illustrates the eDP interface connections. On the left, a blue box represents the eDP panel signals, including EDP\_AUXN, EDP\_AUXP, EDP\_HPD, EDP\_TXN0, EDP\_TXN1, EDP\_TXP0, EDP\_TXP1, EDP\_RCOMP, EDP\_DISP\_UTIL, FDI\_TXN0, FDI\_TXP0, FDI\_TXN1, and FDI\_TXP1. On the right, a red box represents the system signals, including F15, F14, EDP\_HPD#, C14, A12, D14, B12, AG6, EDP\_RCOMP, R204, 24.9R1%0402, +VCCIOA\_OUT, E12, C12, D12, A14, B14, A3, A4, A51, A52, A53, B3, B3X, B52, B53, B54, BC1, BC54, BD1, BD54, BE1, BE2, BE3, BE4, BE5, BF1, BF2, BF3, BF4, BF5. A red oval highlights the FDI signals (FDI\_TXN0, FDI\_TXP0, FDI\_TXN1, FDI\_TXP1) and their corresponding system signals (C12, D12, A14, B14). The text "To eDP Panal" is written in the center. A table at the bottom explains the PCI Express Static x16 Lane Numbering Reversal and the MSR Privacy Bit Feature.

PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden



10 OF 12





## +VCC\_CORE

HASWELL\_BGA\_E

U68E

+VCC\_CORE



+VCC\_CORE



5 OF 12

PEC18



+VCCIO\_OUT



Close to IMVP

VIA\_IVR\_ERROR  
VIA\_ICT\_TRIGGER

Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	1-15
2. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	16-30
3. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	31-45
4. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	46-60
5. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	61-75
6. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	76-90
7. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	91-105
8. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	106-120
9. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	121-135
10. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	136-150

Size

Document Number

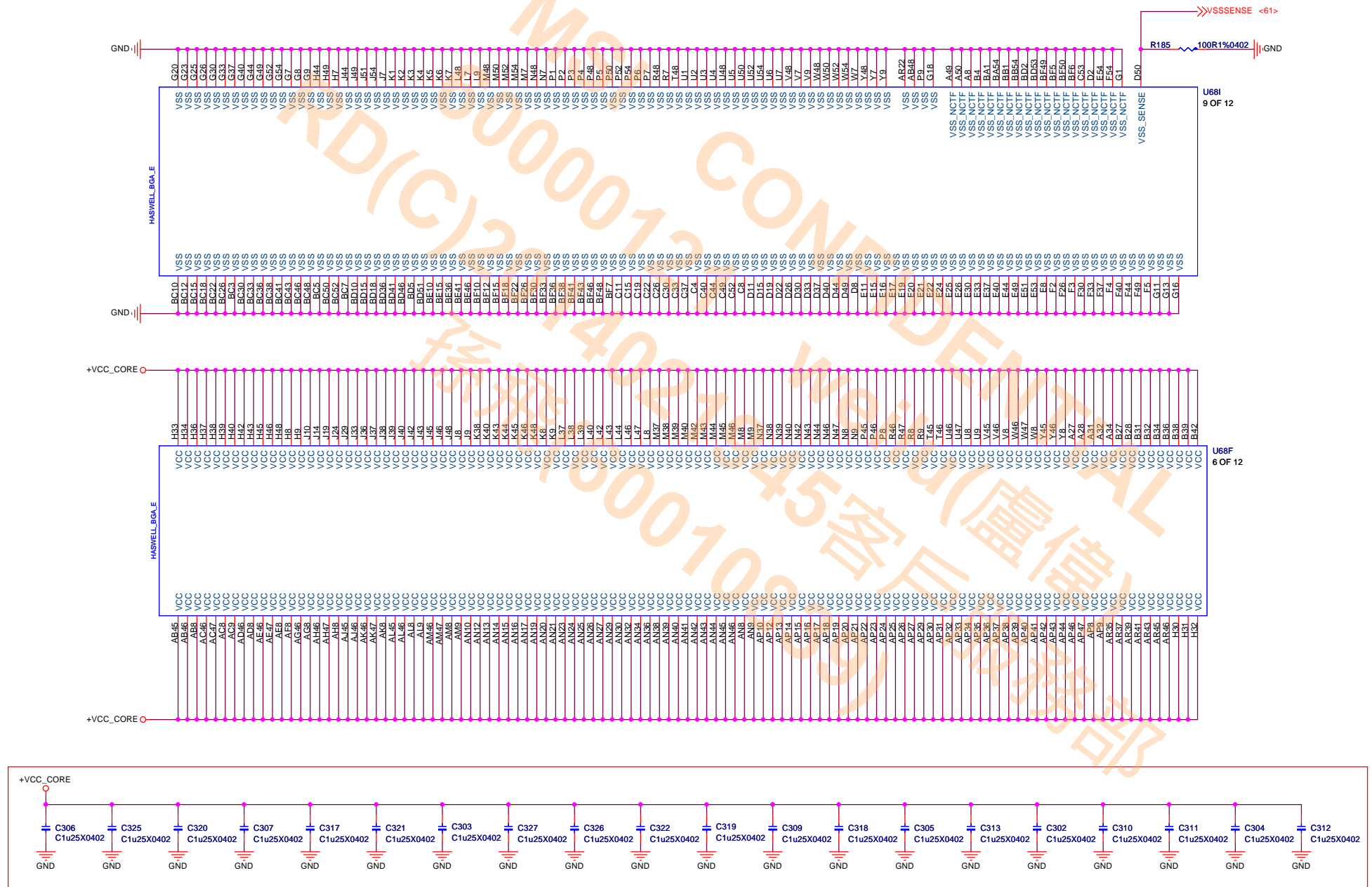
114

MS 1642

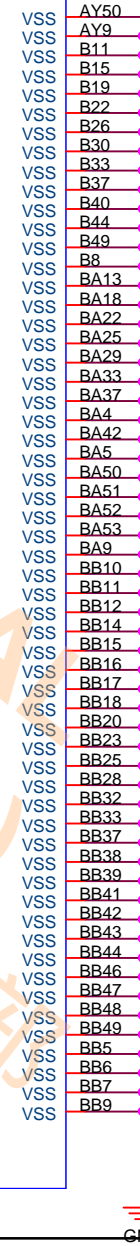
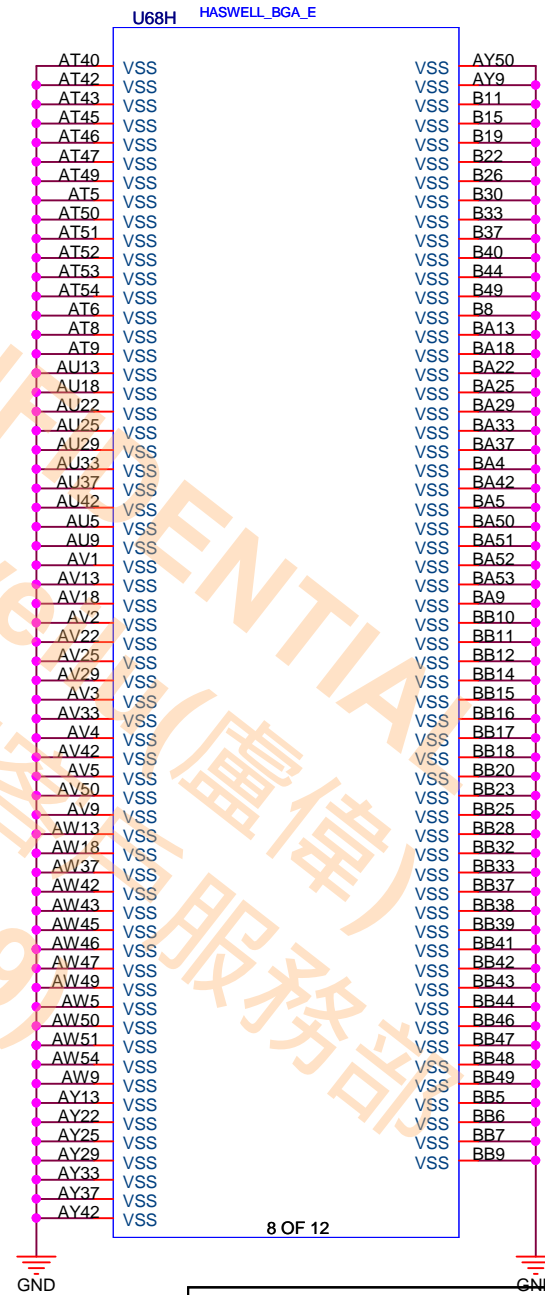
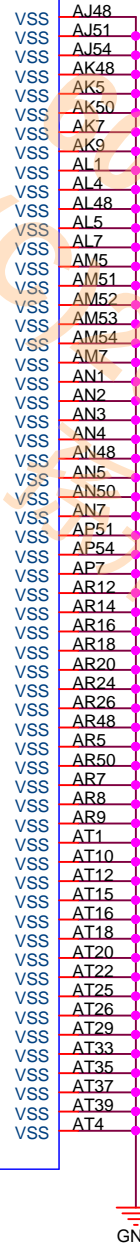
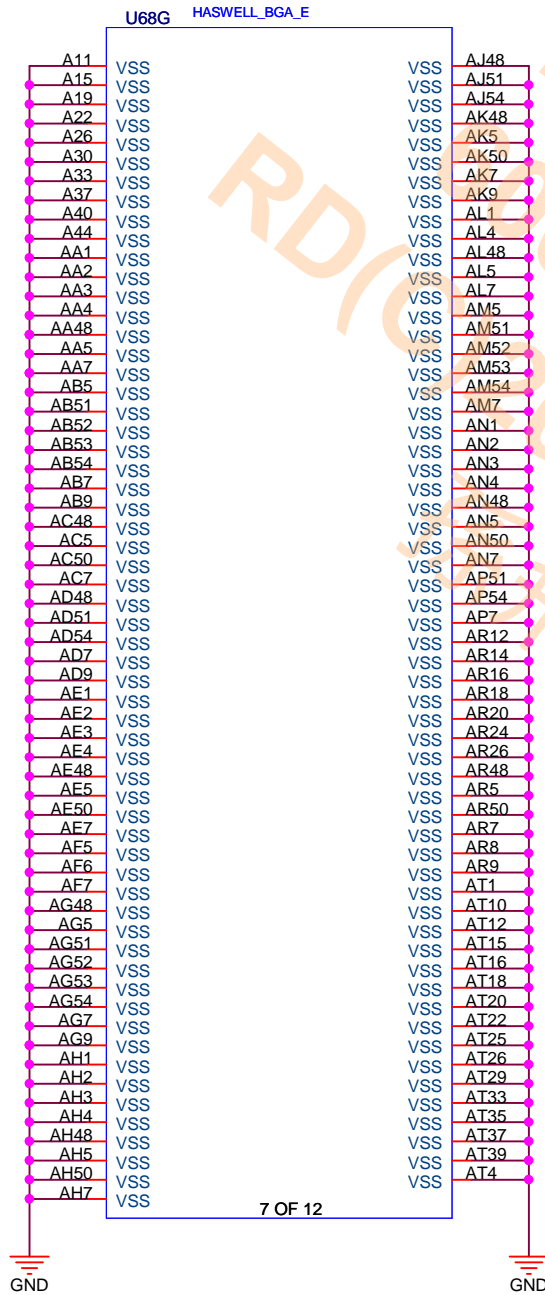
Rev

04

## Haswell ( Power & GND )



# Haswell ( GND )



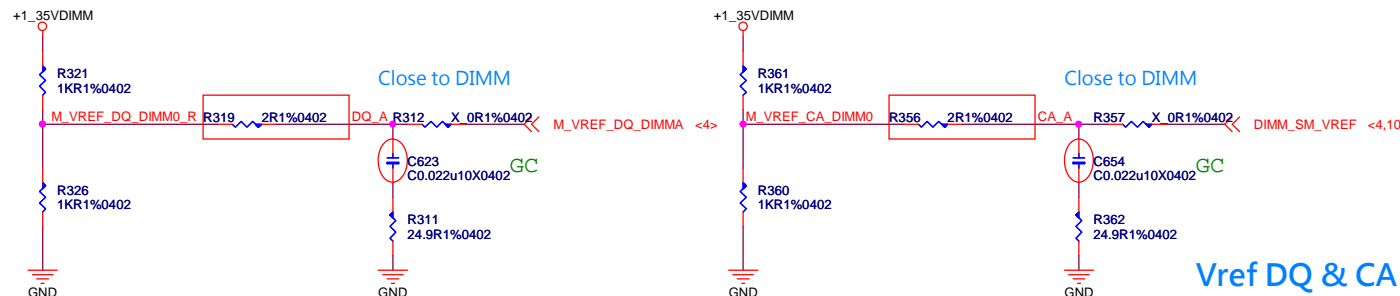
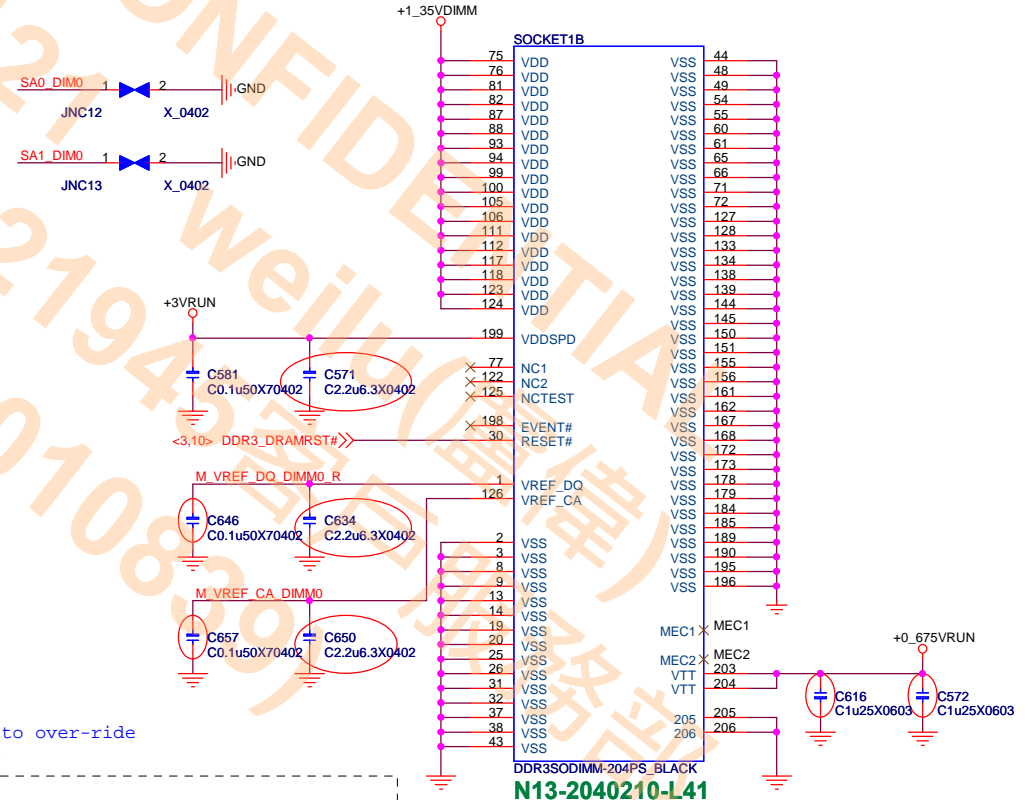
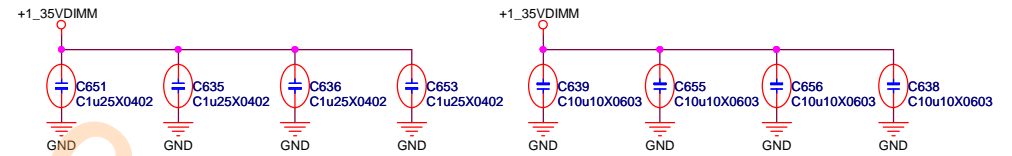
MICRO-STAR INT'L CO.,LTD.

Title		
CPU-5 ( GND )		
Size	Document Number	Rev
	MS-16H2	0A
Date:	Thursday, September 05, 2013	Sheet 8 of 71

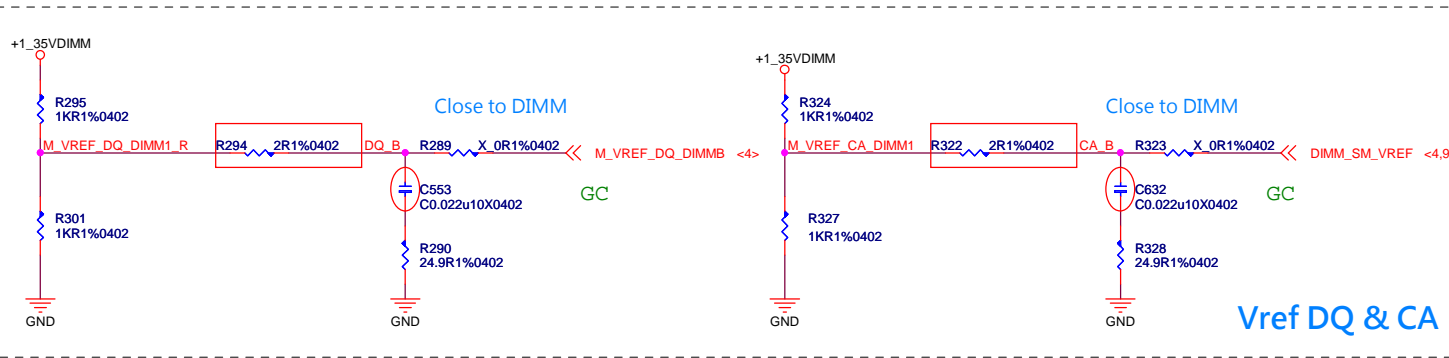
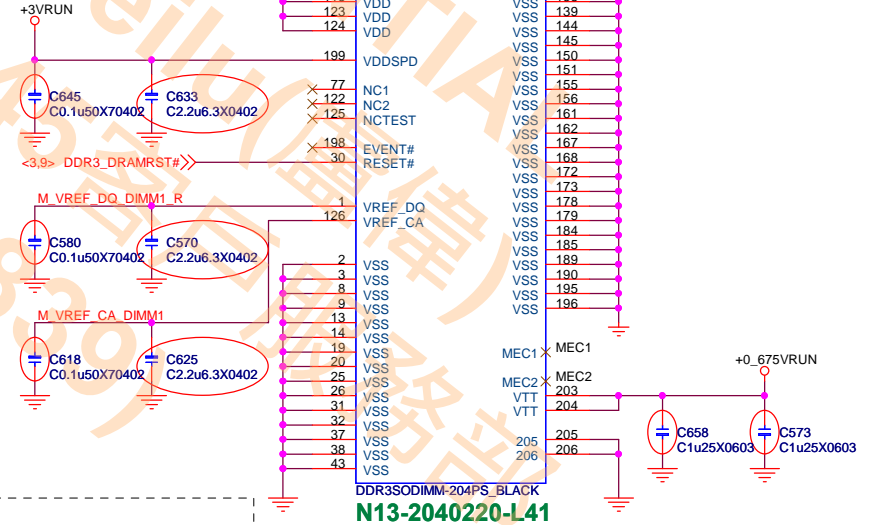
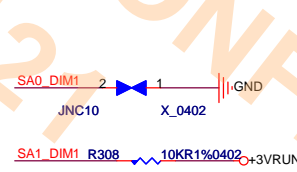
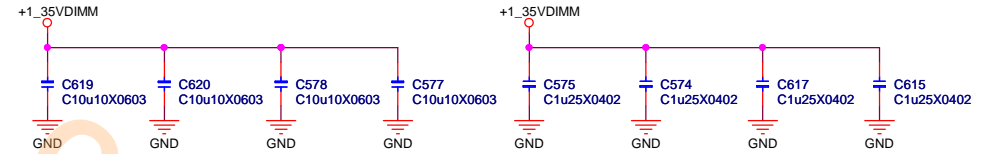
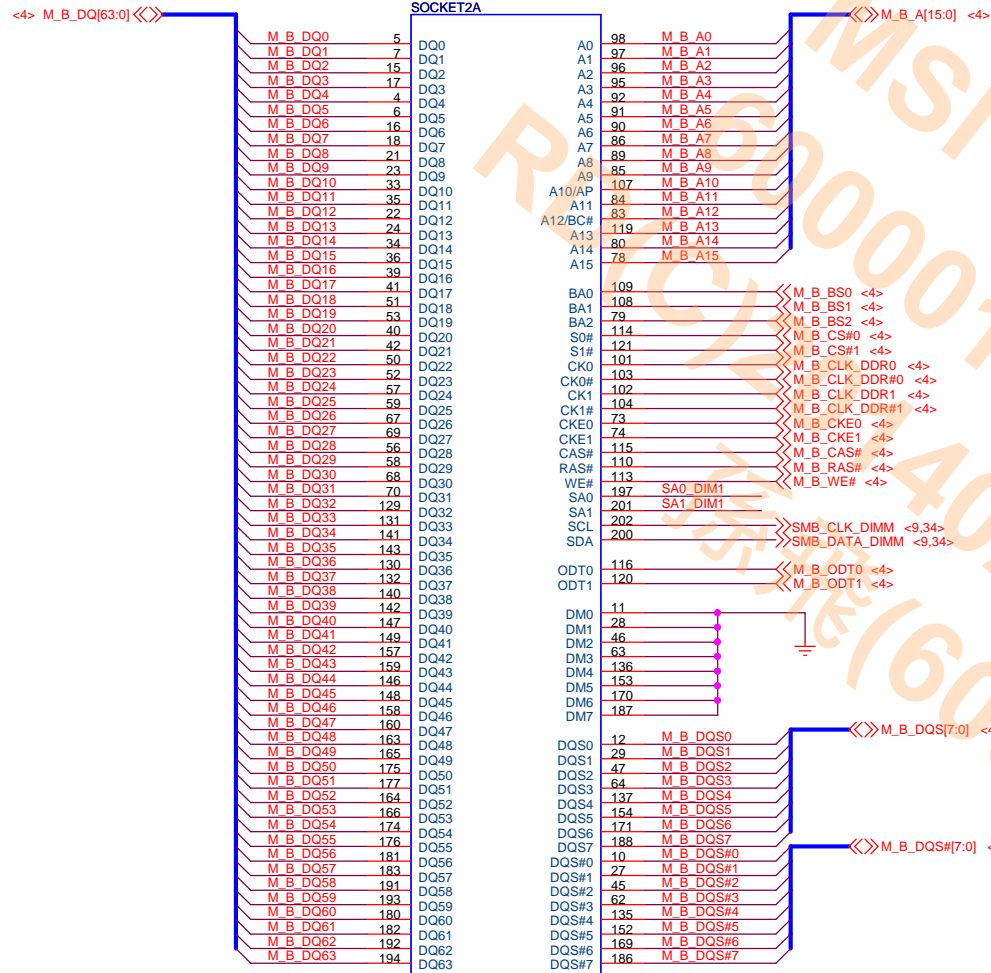


The diagram illustrates the electrical connections for the DIMM0 socket. It shows the following components and connections:

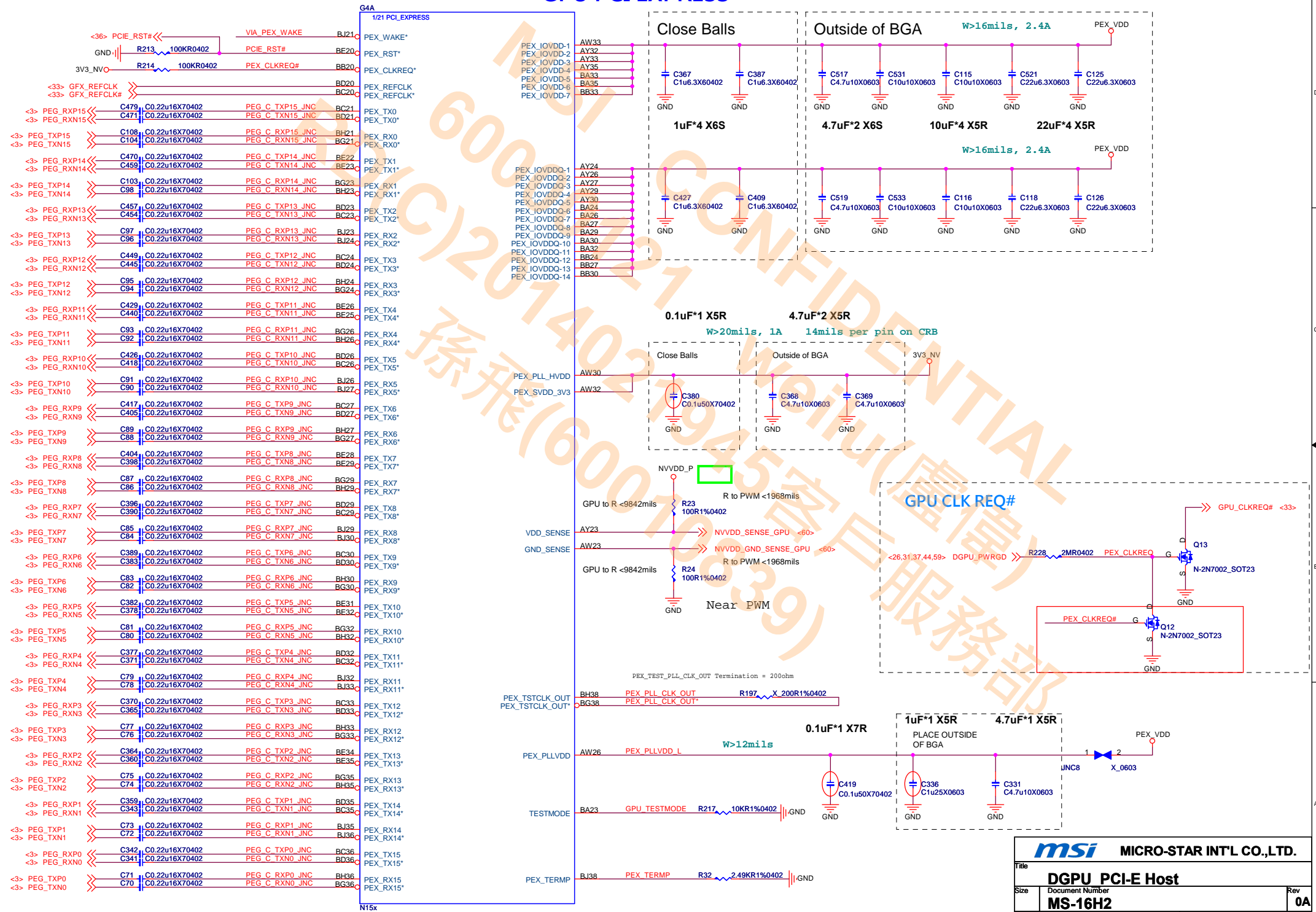
- Power Planes:** +1.35V DIMM, +3V RUN, VREF DO, VREF CA.
- Decoupling Capacitors:** C651, C635, C636, C653, C639, C658, C571, C646, C634, C657, C650.
- Signal Connections:** M\_A, M\_A\_BS, M\_A\_CLK, M\_A\_CKE, M\_A\_CAS, M\_A\_RAS, M\_A\_WE, M\_A\_ODT, M\_A\_DQS, M\_A\_DQS#.
- Socket Connector:** DIMM0, DIMM1, DIMM2, DIMM3, DIMM4, DIMM5, DIMM6, DIMM7.
- Component Values:** C651, C635, C636, C653, C639, C658, C571, C646, C634, C657, C650.



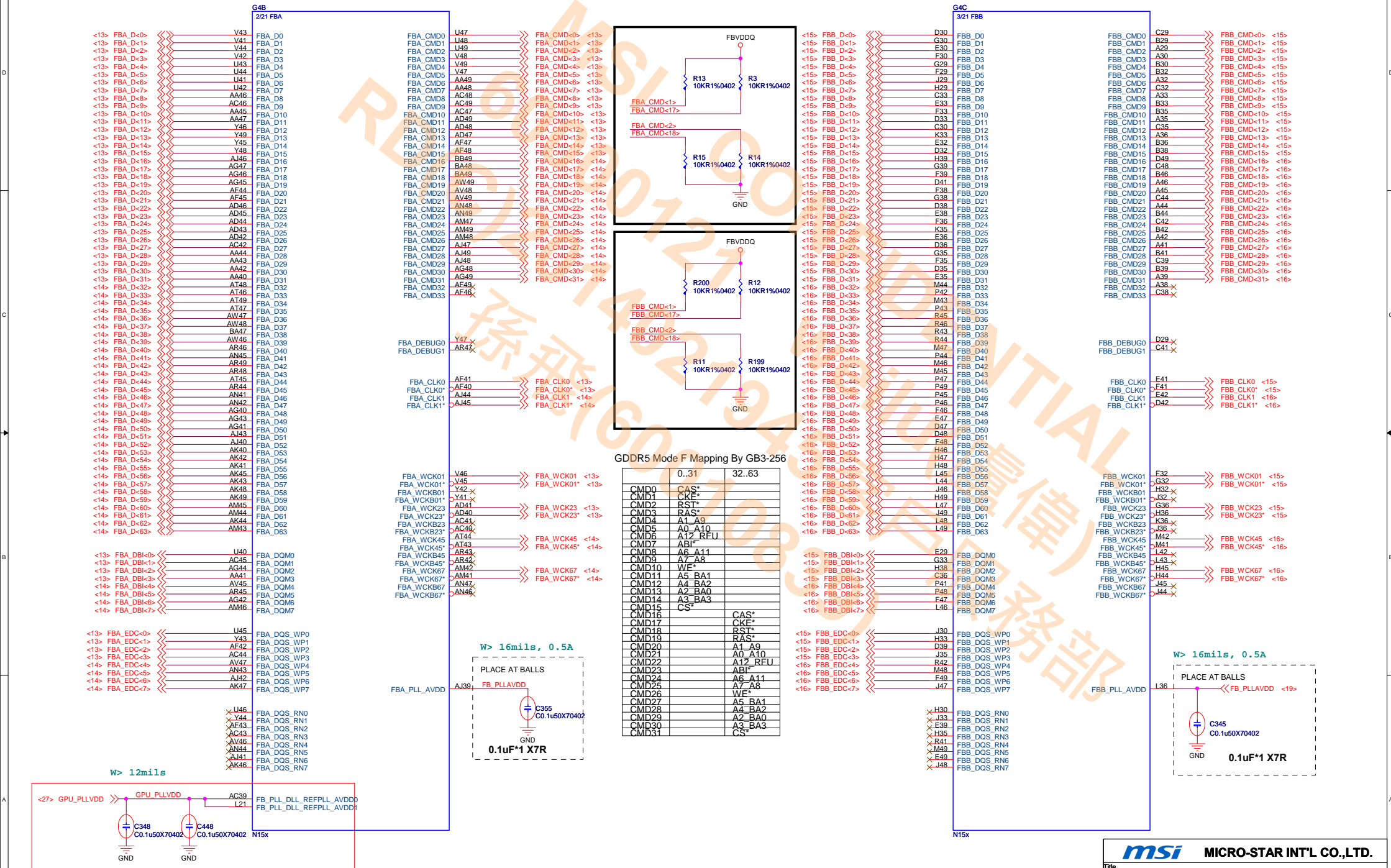
# SODIMM#B



## GPU PCI EXPRESS

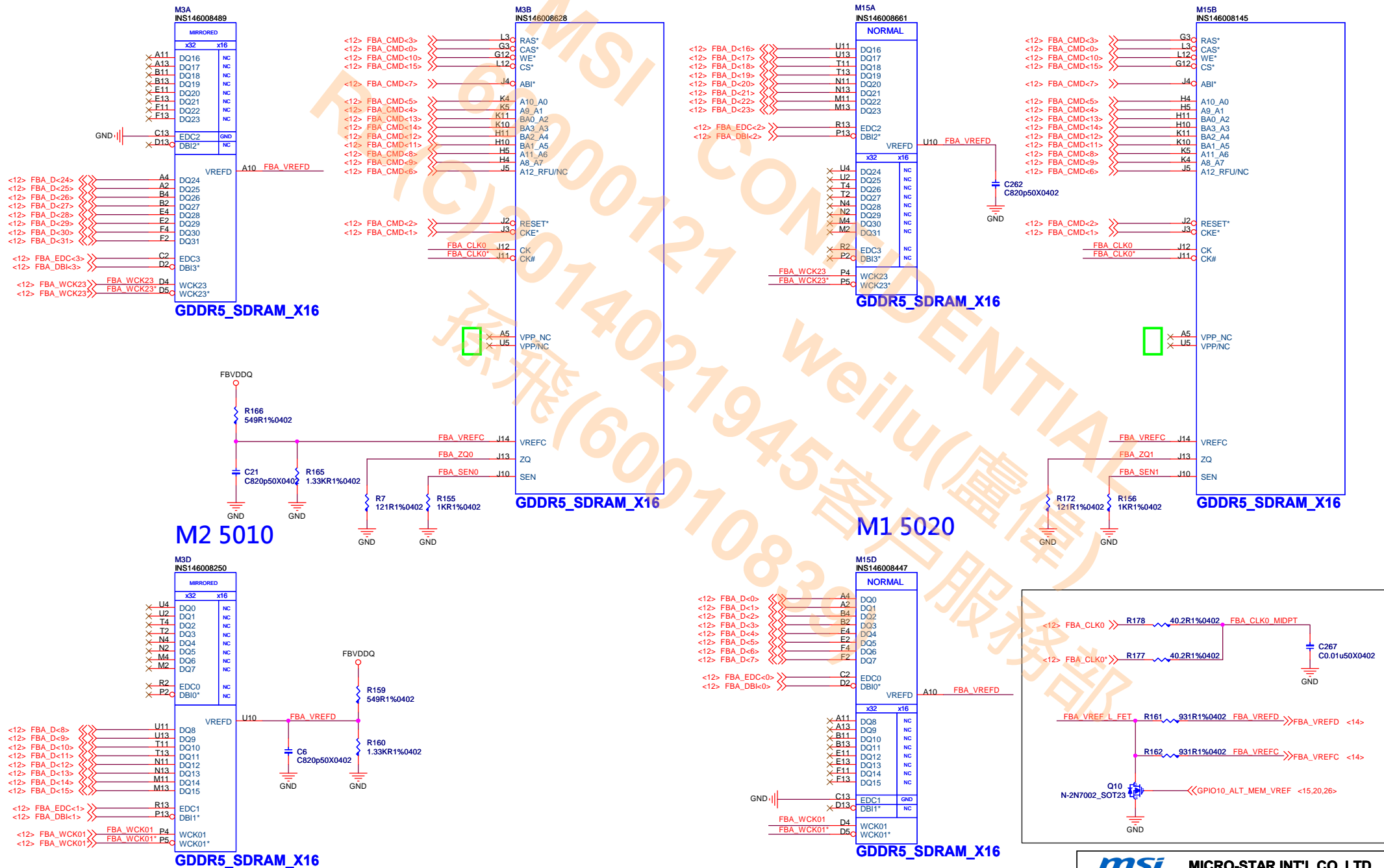


## GPU Frame Buffer Partition A/B



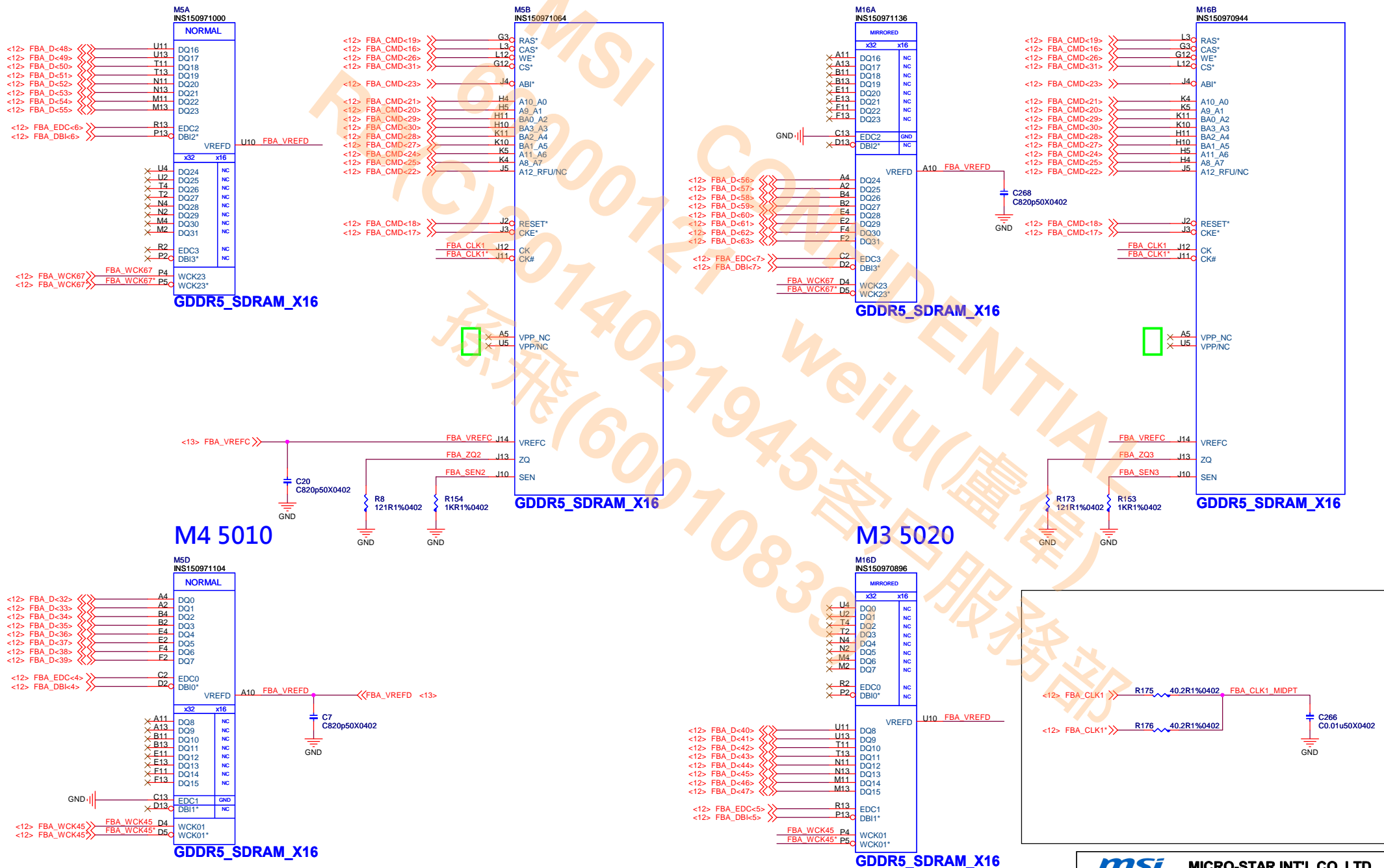


# DGPU\_GDDR5 FrameBuffer A0

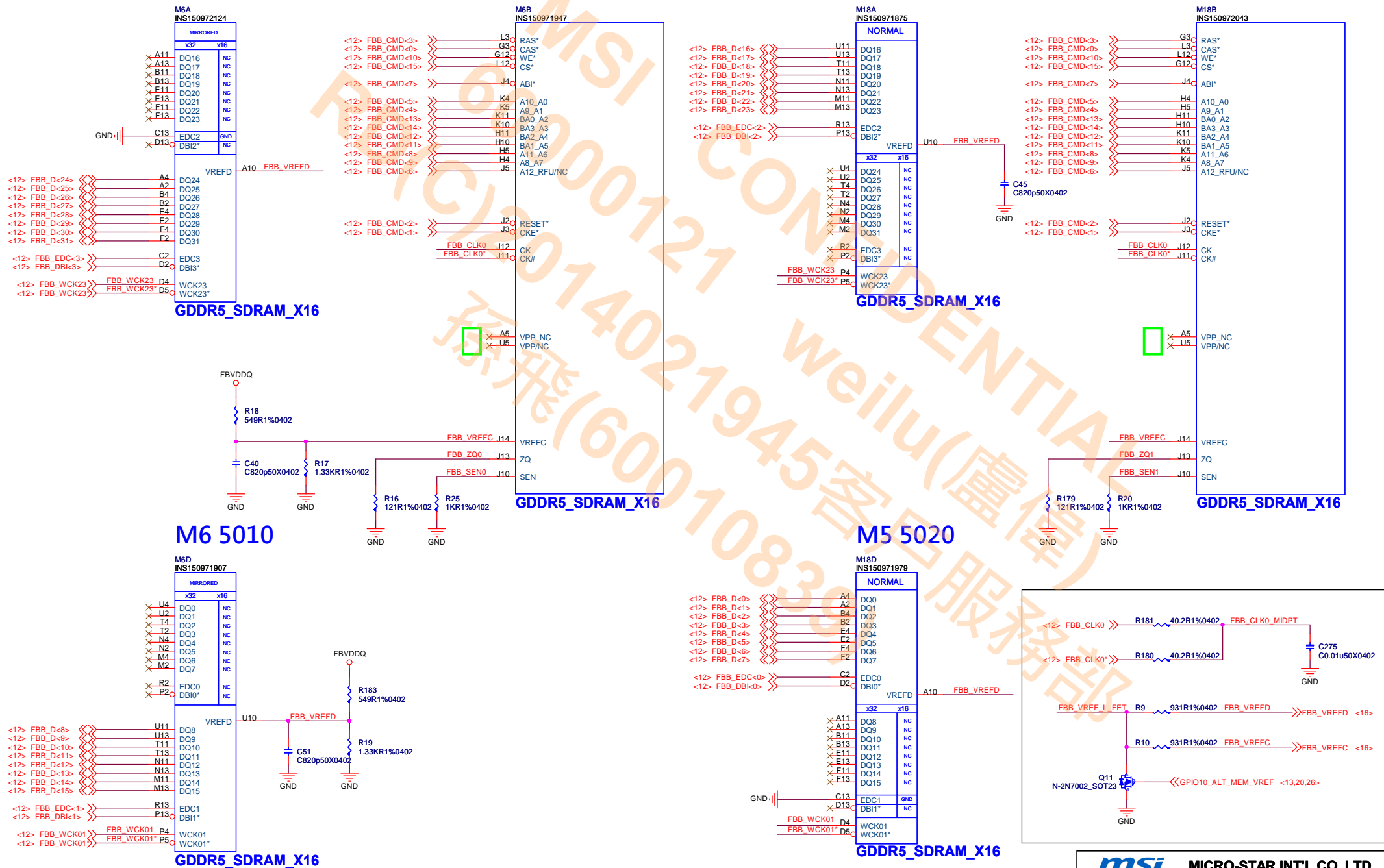




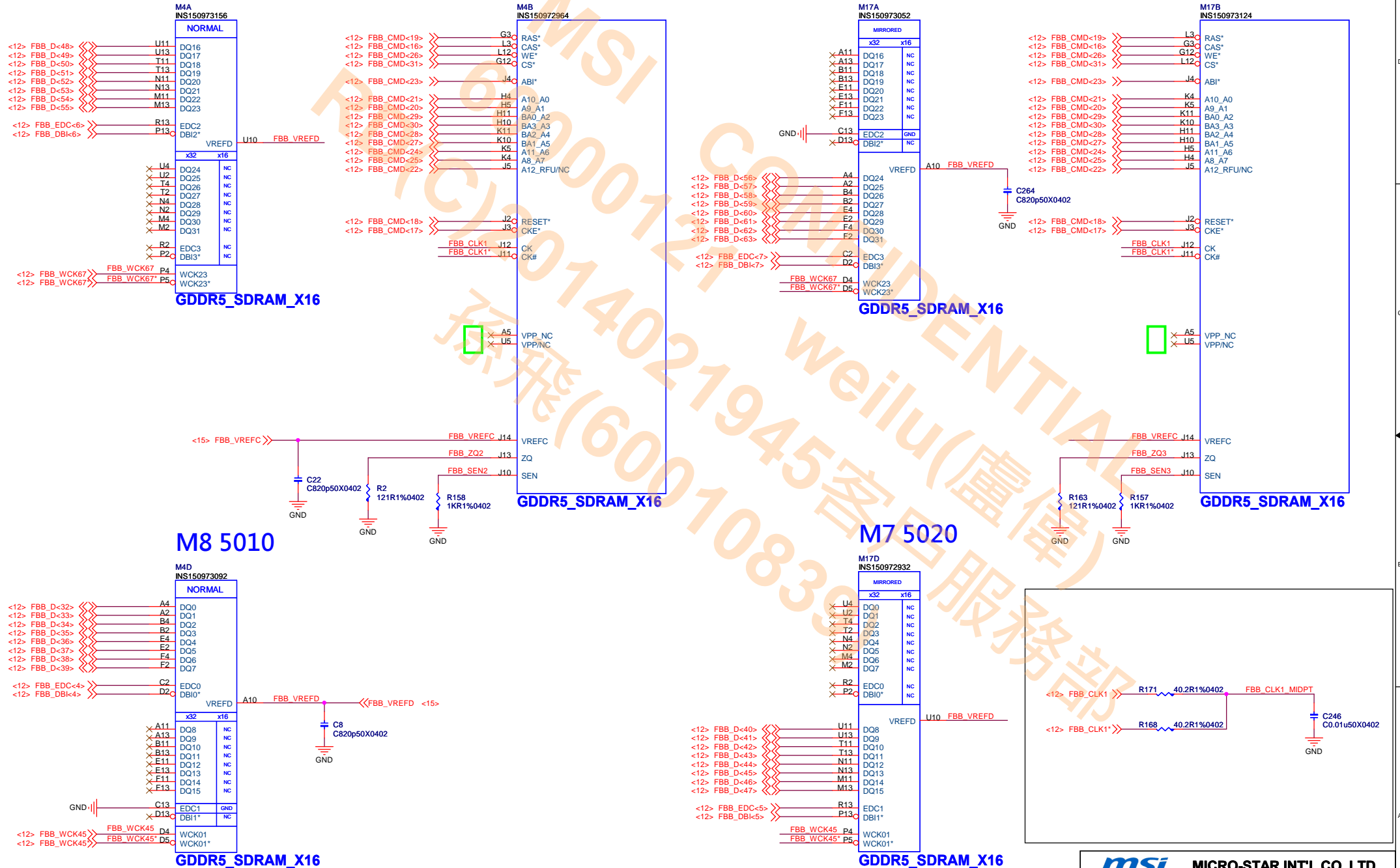
# DGPU\_GDDR5 FrameBuffer A1



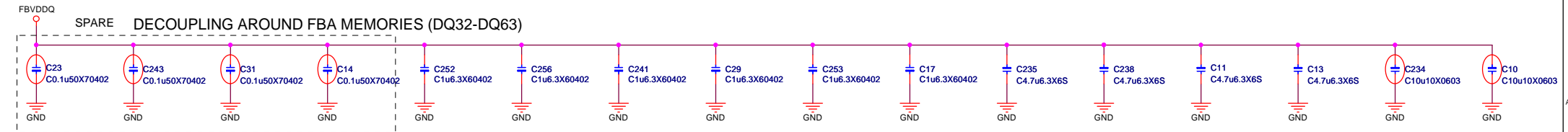
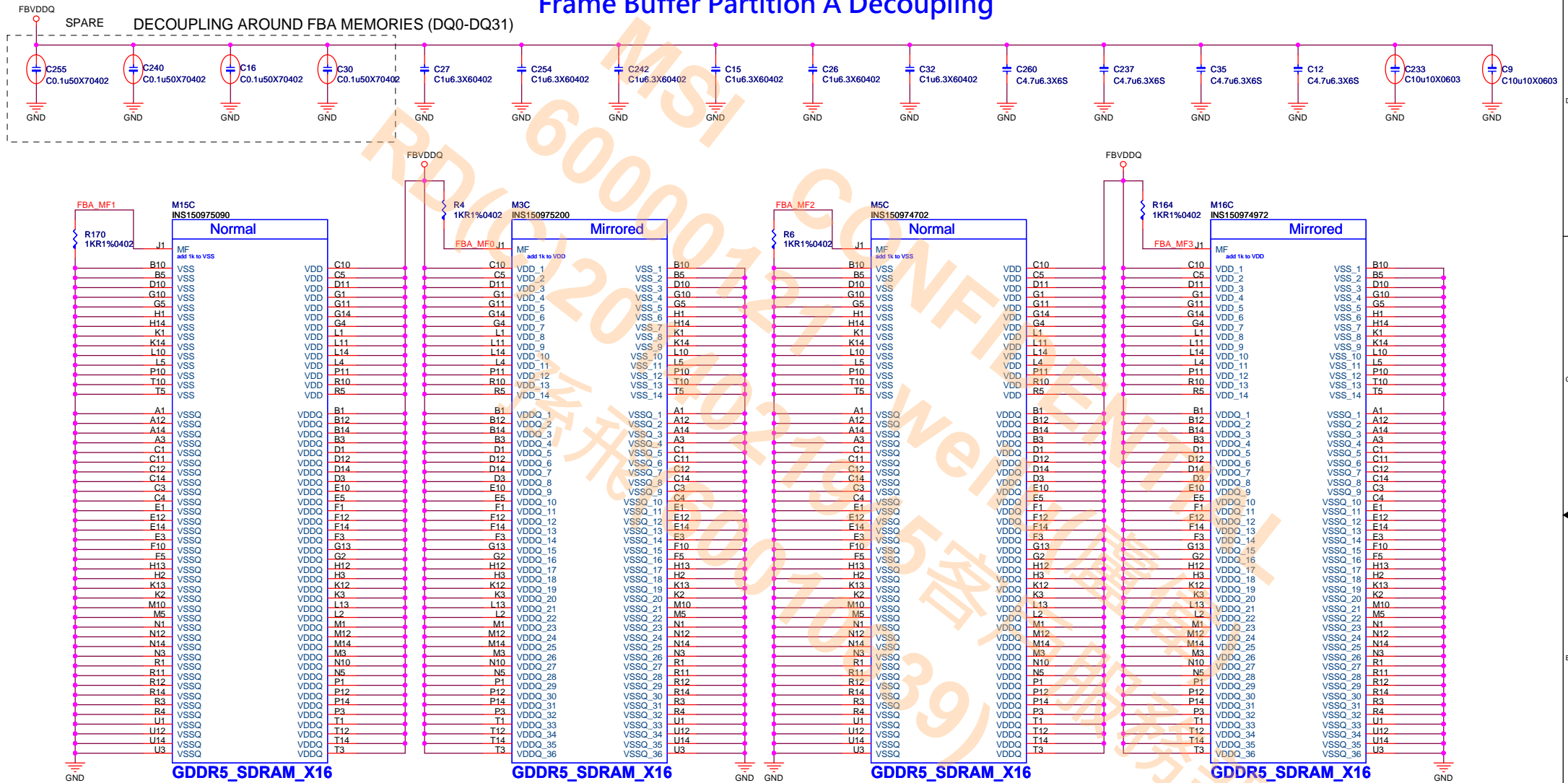
# DGPU\_GDDR5 FrameBuffer B0



# DGPU\_GDDR5 FrameBuffer B1



# Frame Buffer Partition A Decoupling

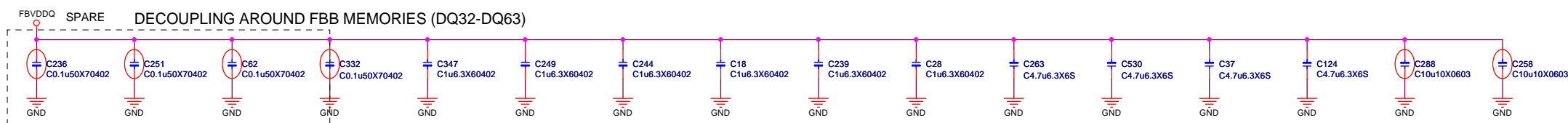


**Frame Buffer Partition B Decoupling**

SPARE DECOUPLING AROUND FBB MEMORIES (DQ0-DQ31)

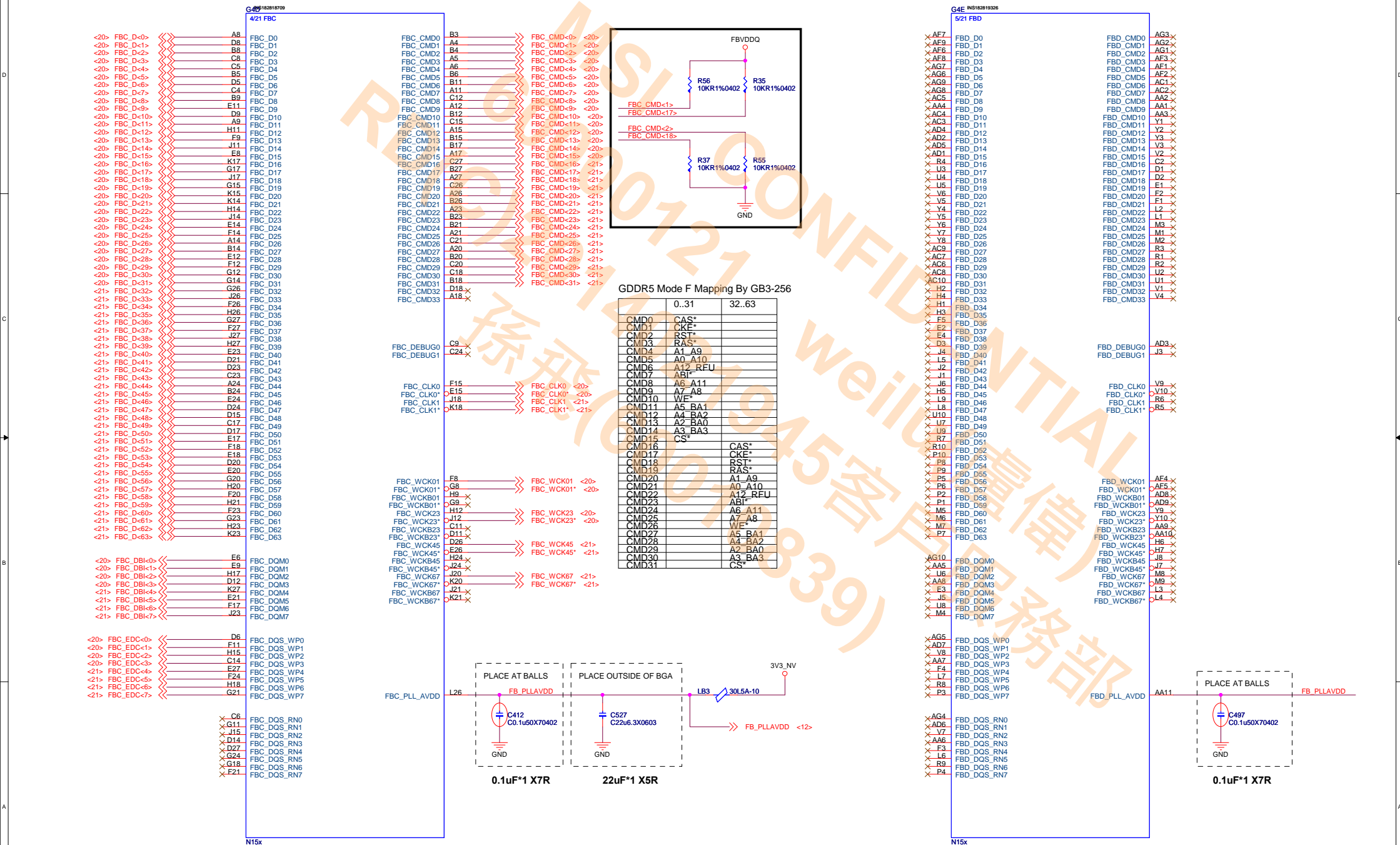
The diagram shows a horizontal bus line representing the DQ0-DQ31 signals. Above the bus, there is a 'SPARE' label and a 'DECOUPLING AROUND FBB MEMORIES (DQ0-DQ31)' label. Below the bus, there are 16 decoupling capacitors, each connected to GND. The capacitors are labeled as follows:

- C272 C0.1u50X70402
- C269 C0.1u50X70402
- C24 C0.1u50X70402
- C19 C0.1u50X70402
- C271 C1u6.3X60402
- C250 C1u6.3X60402
- C245 C1u6.3X60402
- C42 C1u6.3X60402
- C43 C1u6.3X60402
- C39 C1u6.3X60402
- C270 C4.7u6.3X6S
- C261 C4.7u6.3X6S
- C41 C4.7u6.3X6S
- C36 C4.7u6.3X6S
- C257 C10u10X0603
- C492 C10u10X0603

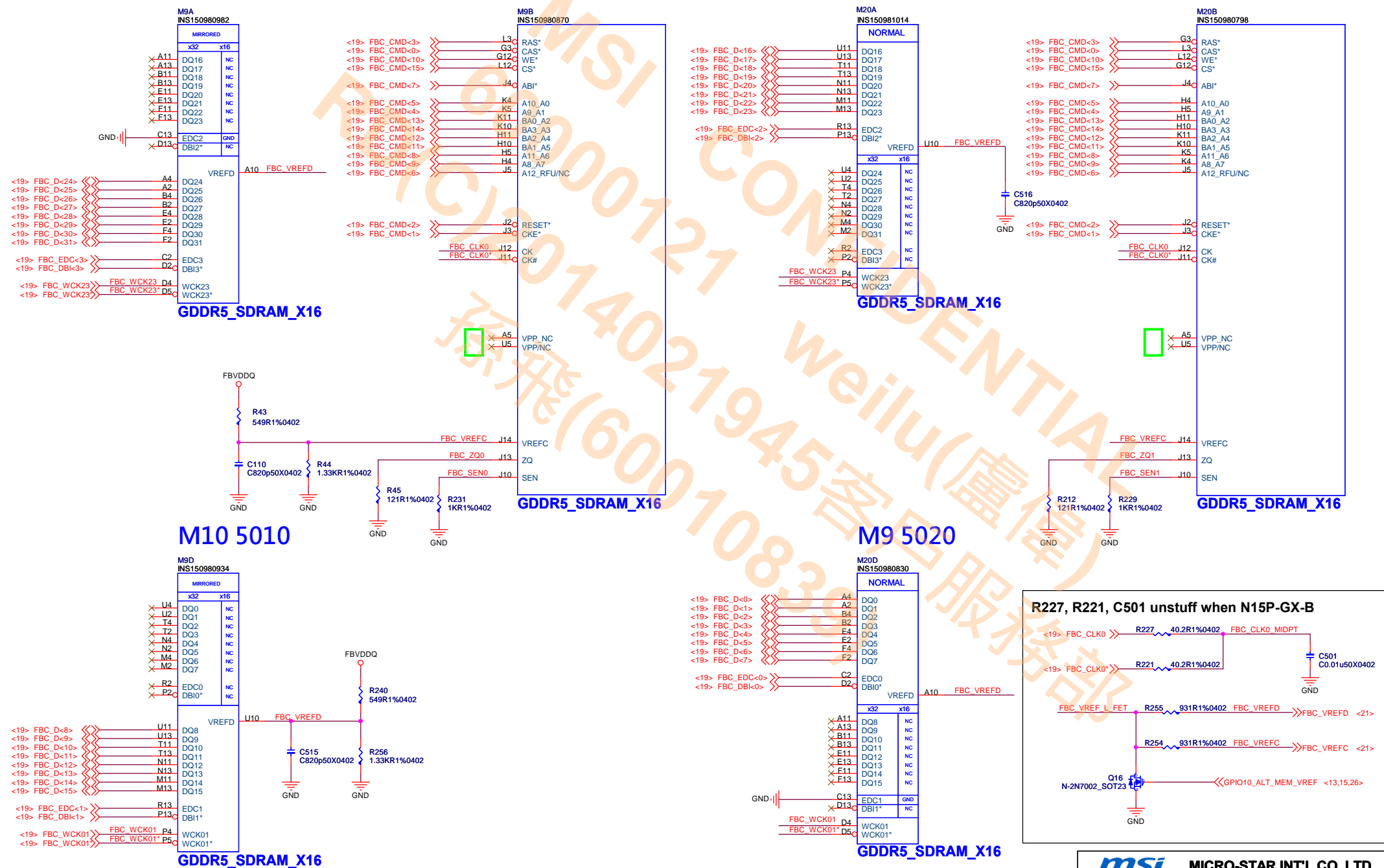




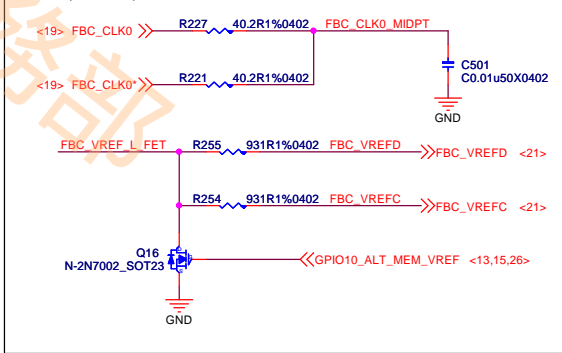
## GPU Frame Buffer Partition C/D



## DGPU\_GDDR5 FrameBuffer C0



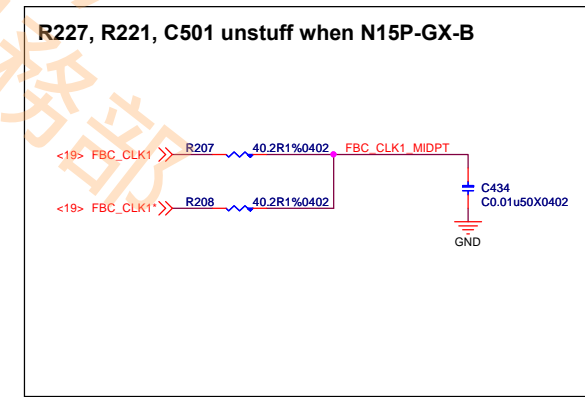
**R227, R221, C501 unstuff when N15P-GX-B**



The diagram illustrates the electrical connections for DDR5 SDRAM components on a PCB. Key components and their connections include:

- M8B M150981804**: A central component with multiple pins connected to various signals.
  - Top Connections**: G3, L3, L12, G12, I4, H4, H5, H11, H10, K11, K10, K5, K4, J5. These are connected to signals like FBC\_CMD<19>, FBC\_CMD<16>, FBC\_CMD<26>, FBC\_CMD<31>, FBC\_CMD<23>, FBC\_CMD<21>, FBC\_CMD<20>, FBC\_CMD<29>, FBC\_CMD<30>, FBC\_CMD<28>, FBC\_CMD<27>, FBC\_CMD<24>, FBC\_CMD<25>, and FBC\_CMD<22>.
  - Bottom Connections**: J2, J3, J12, J11, J10, J13. These are connected to signals like FBC\_CMD<18>, FBC\_CMD<17>, FBC\_CLK1, FBC\_CLK1\*, FBC\_VREFC, FBC\_ZQ, and FBC\_SEN2.
  - Power/Ground Connections**: A5, U5, VPP\_NC, VPP/NC, GND.
- GDDR5\_SDRAM\_X16**: A component with pins connected to signals like FBC\_D<56>, FBC\_D<57>, FBC\_D<58>, FBC\_D<59>, FBC\_D<60>, FBC\_D<61>, FBC\_D<62>, FBC\_D<63>, FBC\_EDC<7>, and FBC\_DBI<7>.
- GDDR5\_SDRAM\_X16**: A component with pins connected to signals like FBC\_WCK67, FBC\_WCK67\*, FBC\_DBI2, and FBC\_DBI2\*.
- M11 5020**: A component with pins connected to signals like FBC\_DBI2, FBC\_DBI2\*, FBC\_DBI2, and FBC\_DBI2\*.

The diagram also shows various power and ground connections, including VPP, VREFC, ZQ, SEN, and GND. The layout is labeled with component names and pin numbers.



SPARE

DECOUPLING AROUND FBC MEMORIES (DQ0-DQ31)

Frame Buffer Partition C Decoupling

C333 C0.1u50X70402

C337 C0.1u50X70402

C99 C0.1u50X70402

C102 C0.1u50X70402

C338 C1u6.3X60402

C461 C1u6.3X60402

C462 C1u6.3X60402

C68 C1u6.3X60402

C69 C1u6.3X60402

C61 C1u6.3X60402

C335 C4.7u6.3X6S

C65 C4.7u6.3X6S

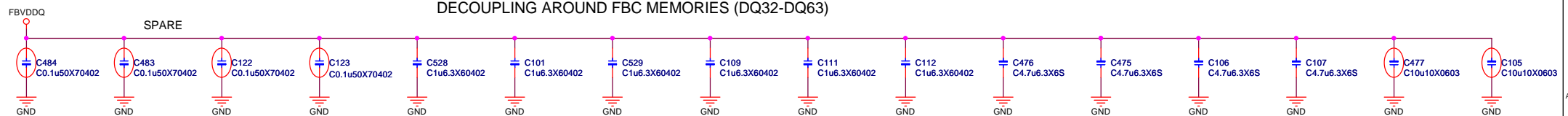
C67 C4.7u6.3X6S

C64 C4.7u6.3X6S

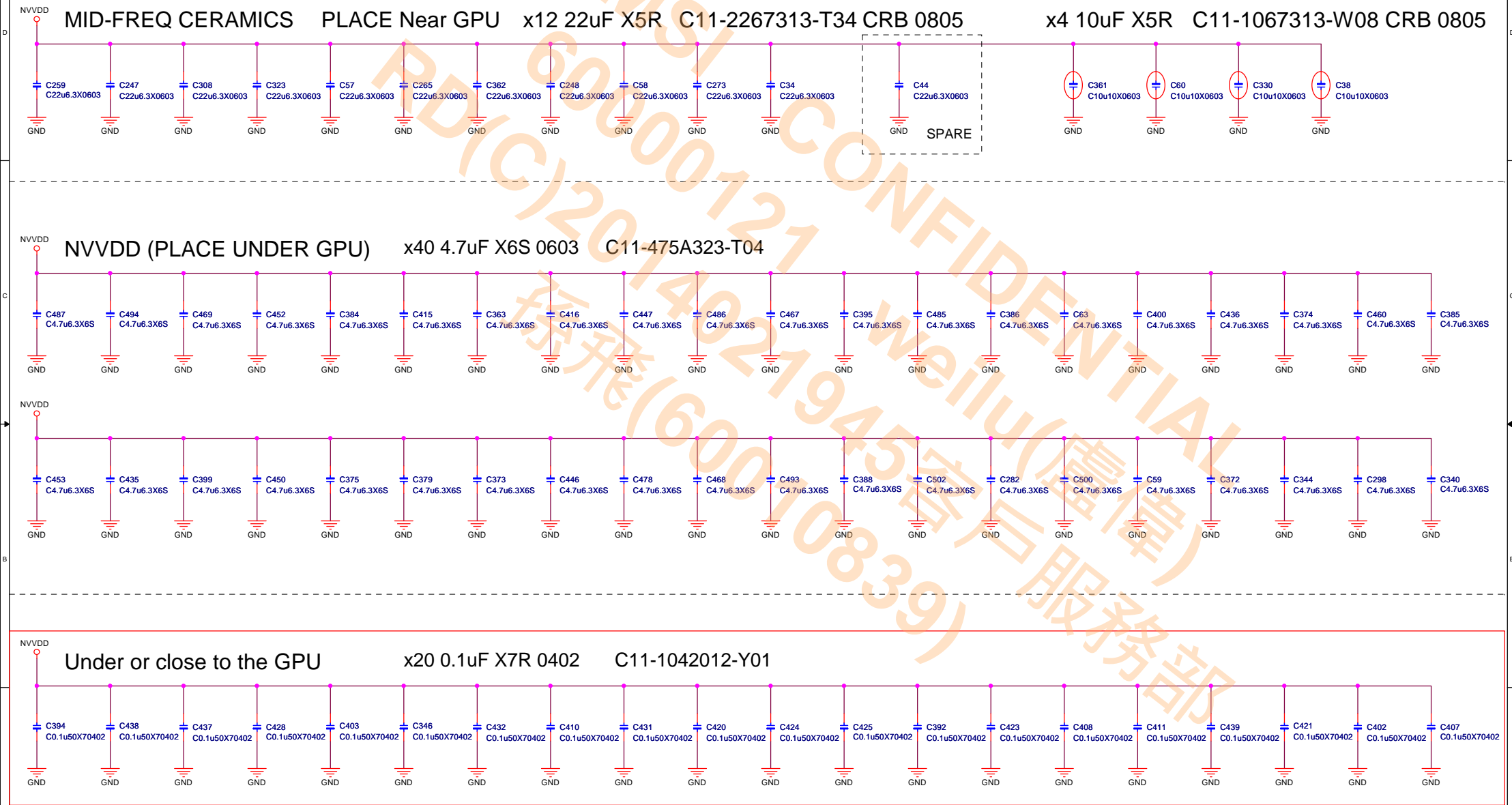
C334 C10u10X0603

C66 C10u10X0603

GND

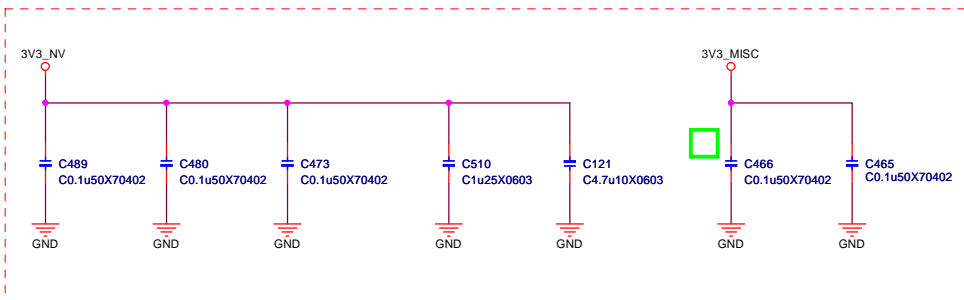
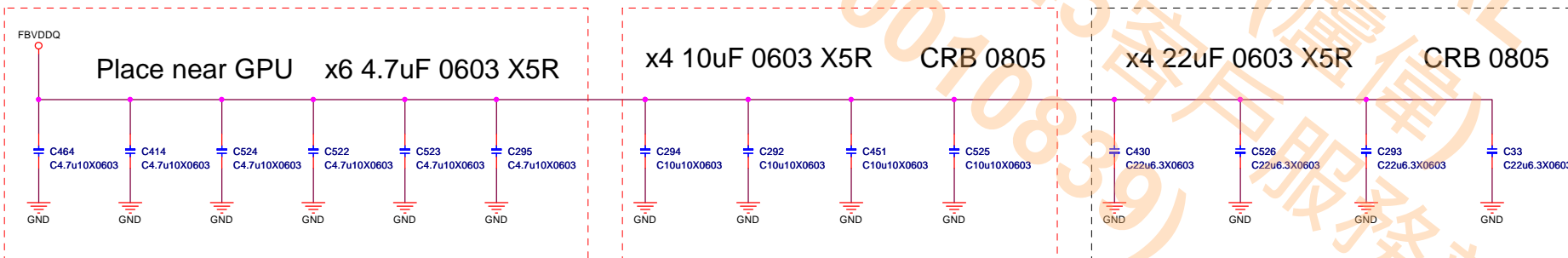
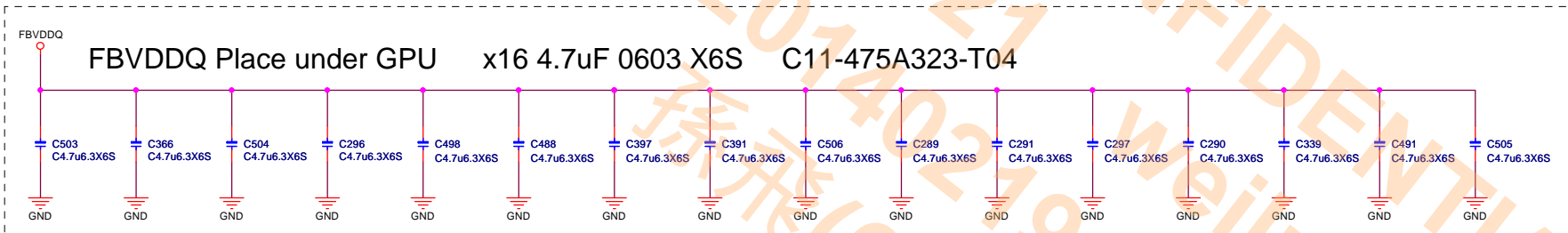
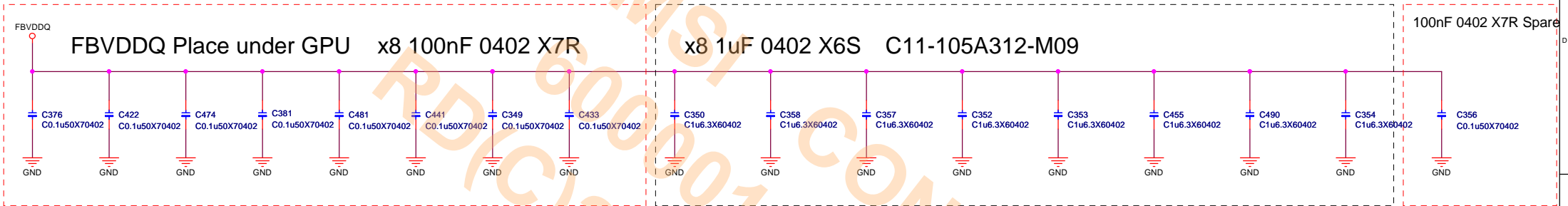


# GPU DECOUPLING A

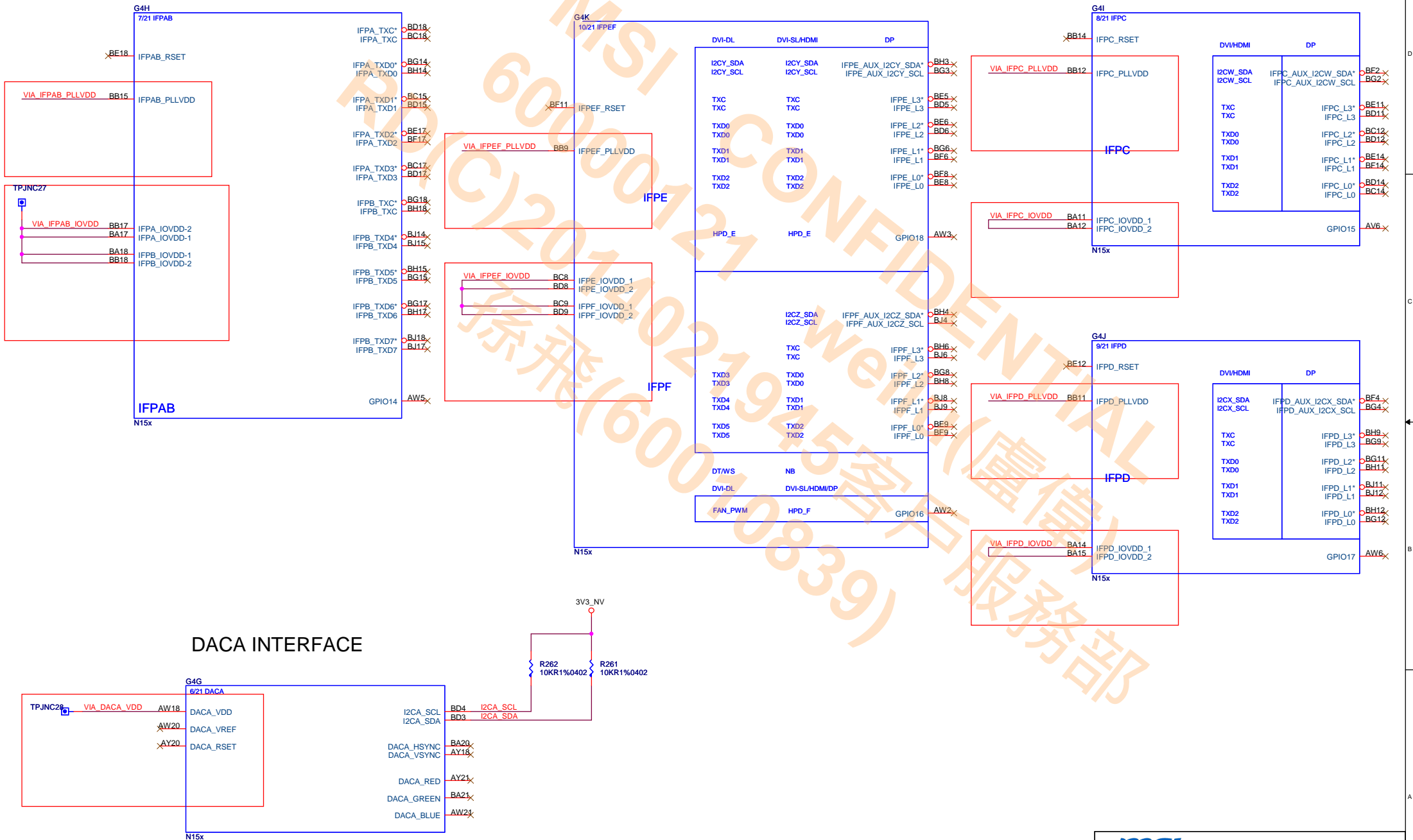




# GPU DECOUPLING B



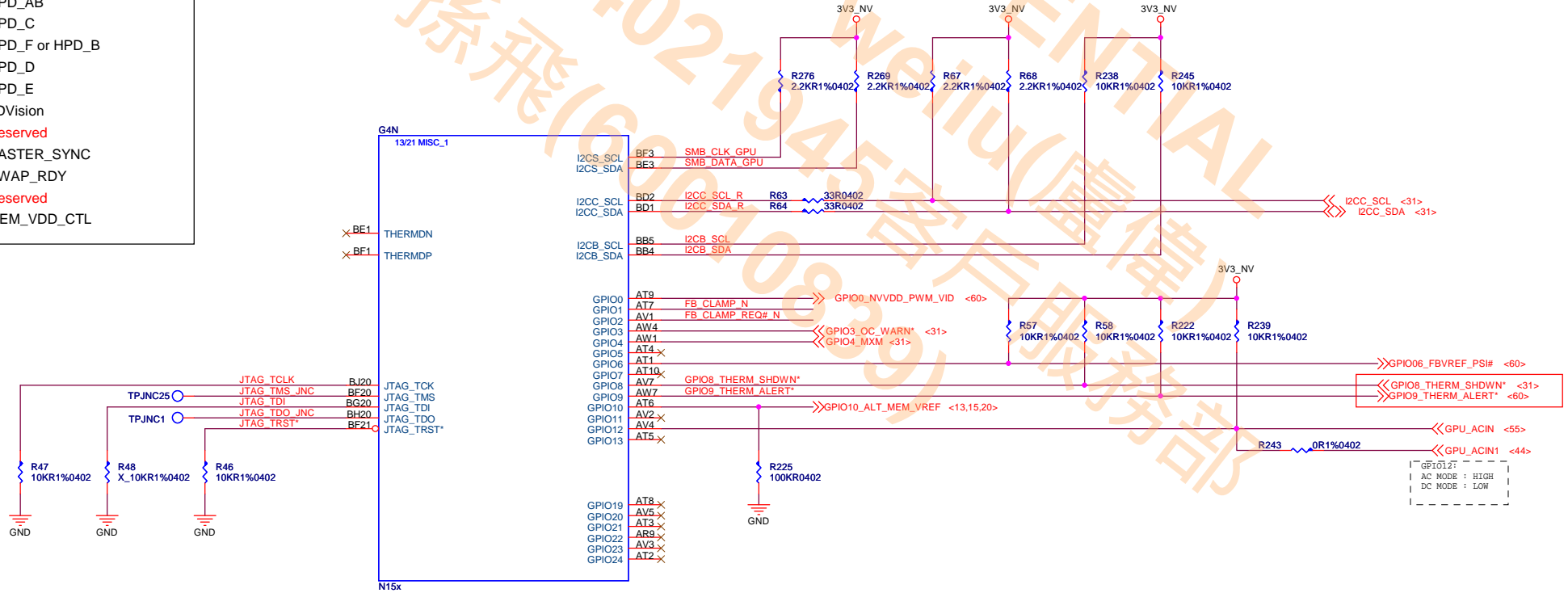
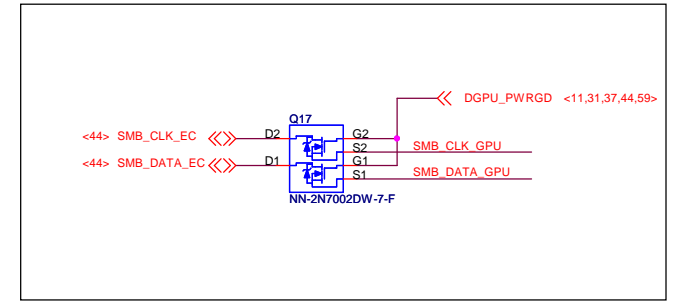
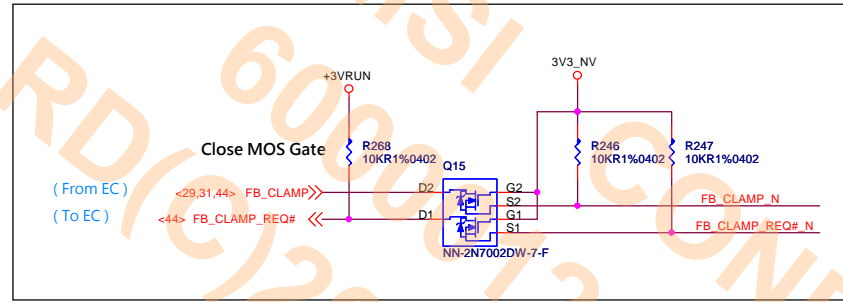
# DACA,Display IF



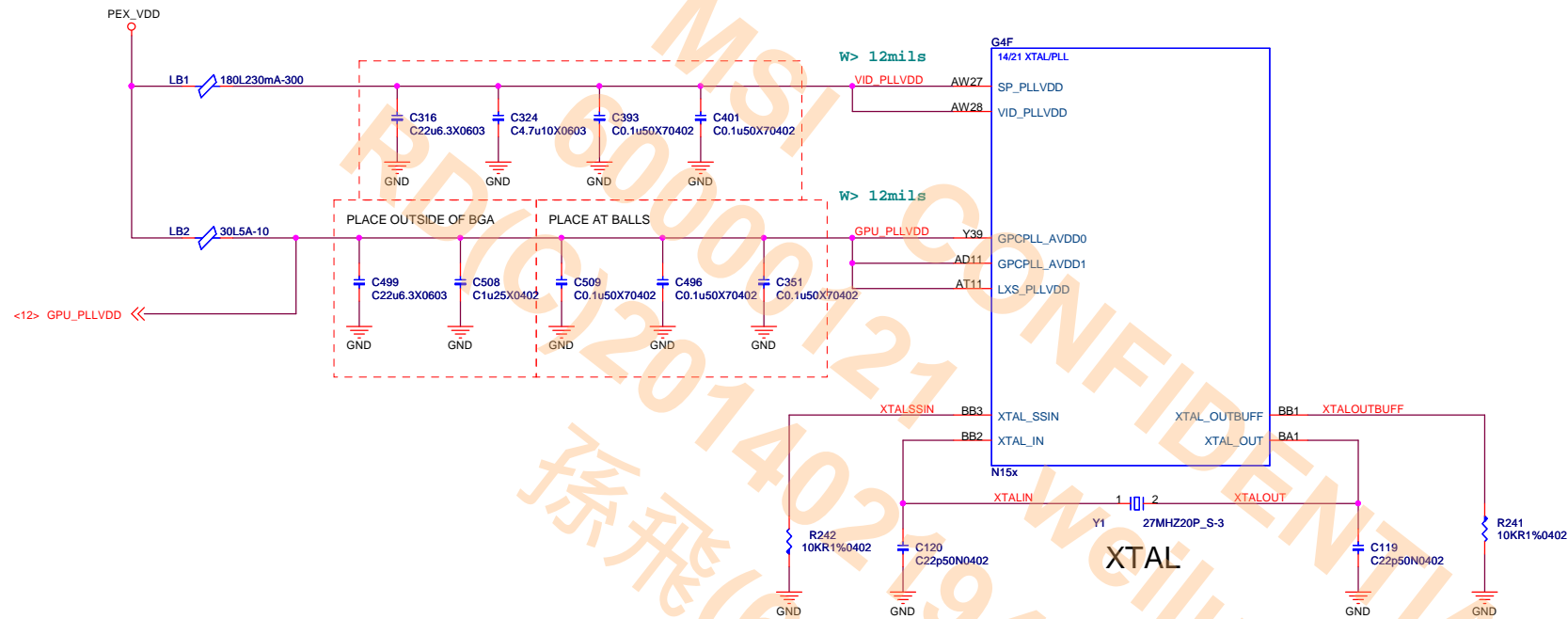
# DGPU GPIO, I2C

GB3-256 GPIO(Design Guide Table 12-2)

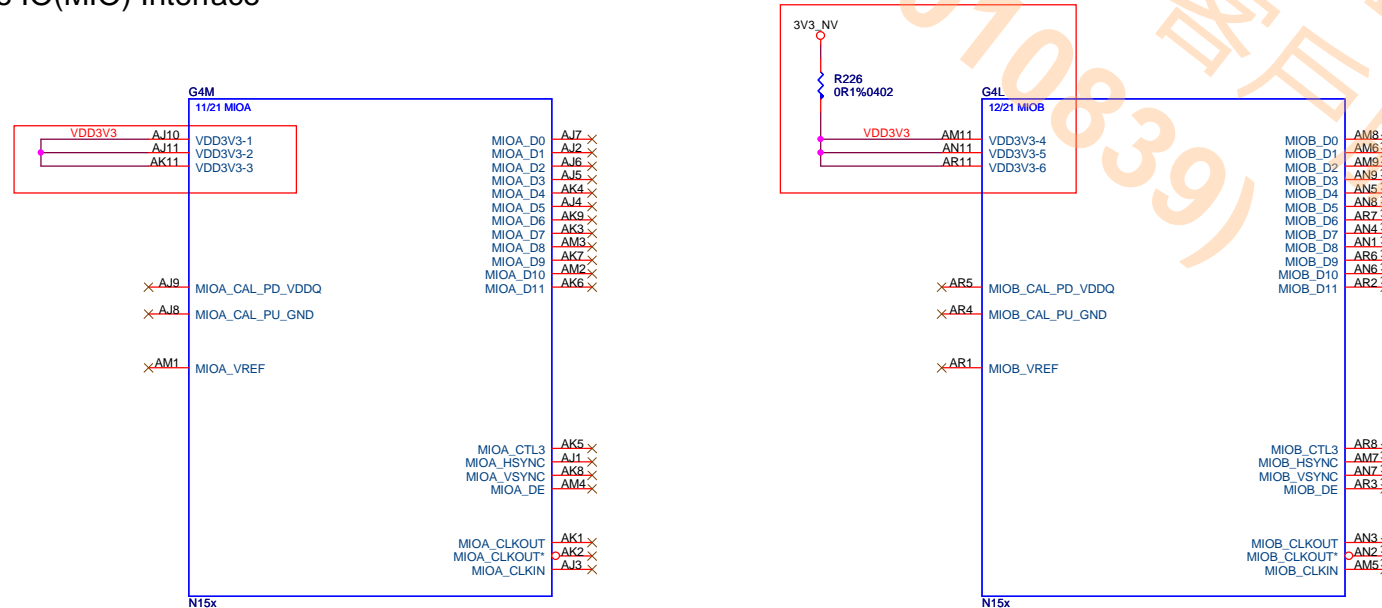
GPIO	I/O	Function
0	OUT	PWM VID
1	IN	FB_CLAMP_MON
2	OUT	FB_CLAMP_MON_TGL_REQ
3	IN	OC_WARN
4	N/A	Reserved
5	N/A	Reserved
6	OUT	PSI
7	OUT	LCD PWM
8	OUT	OVERT
9	I/O	ALERT
10	OUT	MEM_VREF_CTL
11	OUT	LCD_VCC
12	IN	PWM LEVEL
13	OUT	LCD_BLEN
14	IN	HPD_AB
15	IN	HPD_C
16	IN	HPD_F or HPD_B
17	IN	HPD_D
18	IN	HPD_E
19	OUT	3DVision
20	N/A	Reserved
21	I/O	RASTER_SYNC
22	IN	SWAP_RDY
23	N/A	Reserved
24	OUT	MEM_VDD_CTL



# DGPU MIO & XTAL

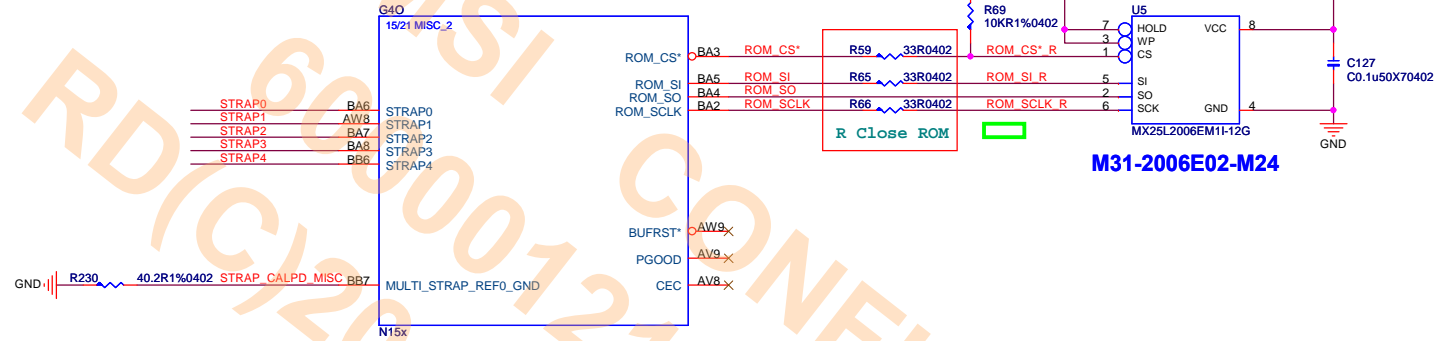


## Multi-use IO(MIO) Interface



# ROM, MULTI-LEVEL STRAPS

GND	3V3
5K	0000
10K	0001
15K	0010
20K	0011
25K	0100
30K	0101
35K	0110
45K	0111
PD	PU

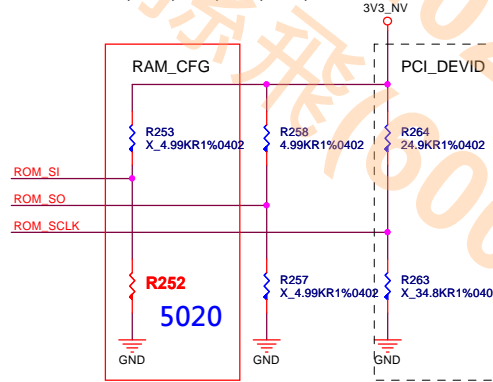


M31-2006E02-M24

RCFG1 Hynix 128Mx16bit R11-3482T12-W08 X_34.8KR1%0402	GDDR5M1 5010 M12-5GQ2HL5-H23 X_H5GQ2H24AFR	GDDR5M2 5020 M12-5GQ2HL5-H23 X_H5GQ2H24AFR
RCFG2 Samsung 128Mx16bit R11-4532T12-W08 X_45.3KR1%0402	GDDR5M3 5010 M12-2032585-S02 X_K4G20325FD	GDDR5M4 5020 M12-2032585-S02 X_K4G20325FD
RCFG3 Hynix 256Mx16bit R11-0153T12-W08 X_15KR1%0402	GDDR5M5 5010 M12-5GC4H05-H23 X_H5GC4H24MFR	GDDR5M6 5020 M12-5GC4H05-H23 X_H5GC4H24MFR
RCFG4 Elpida 256Mx16bit R11-0103T12-W08 X_10KR1%0402	GDDR5M7 5010 M12-4032B05-E59 X_EDW4032BABG	GDDR5M8 5020 M12-4032B05-E59 X_EDW4032BABG

## GDDR5 Parts

5020 : M15, M16, M17, M18, M19, M20  
5010 : M3, M4, M5, M6, M8, M9



## R252

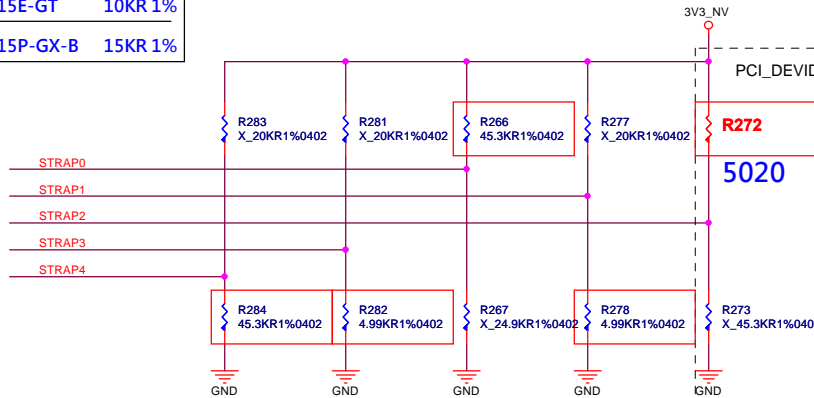
For Hynix 128Mx16 35KR 1%  
For Samsung 128Mx16 45KR 1%  
For Hynix 256Mx16 15KR 1%  
For Elpida 256Mx16 10KR 1%

## Setting

Setting	R252	5010	5020
Hynix 128Mx16	RCFG1	GDDR5M1	GDDR5M2
Samsung 128Mx16	RCFG2	GDDR5M3	GDDR5M4
Hynix 256Mx16	RCFG3	GDDR5M5	GDDR5M6
Elpida 256Mx16	RCFG4	GDDR5M7	GDDR5M8

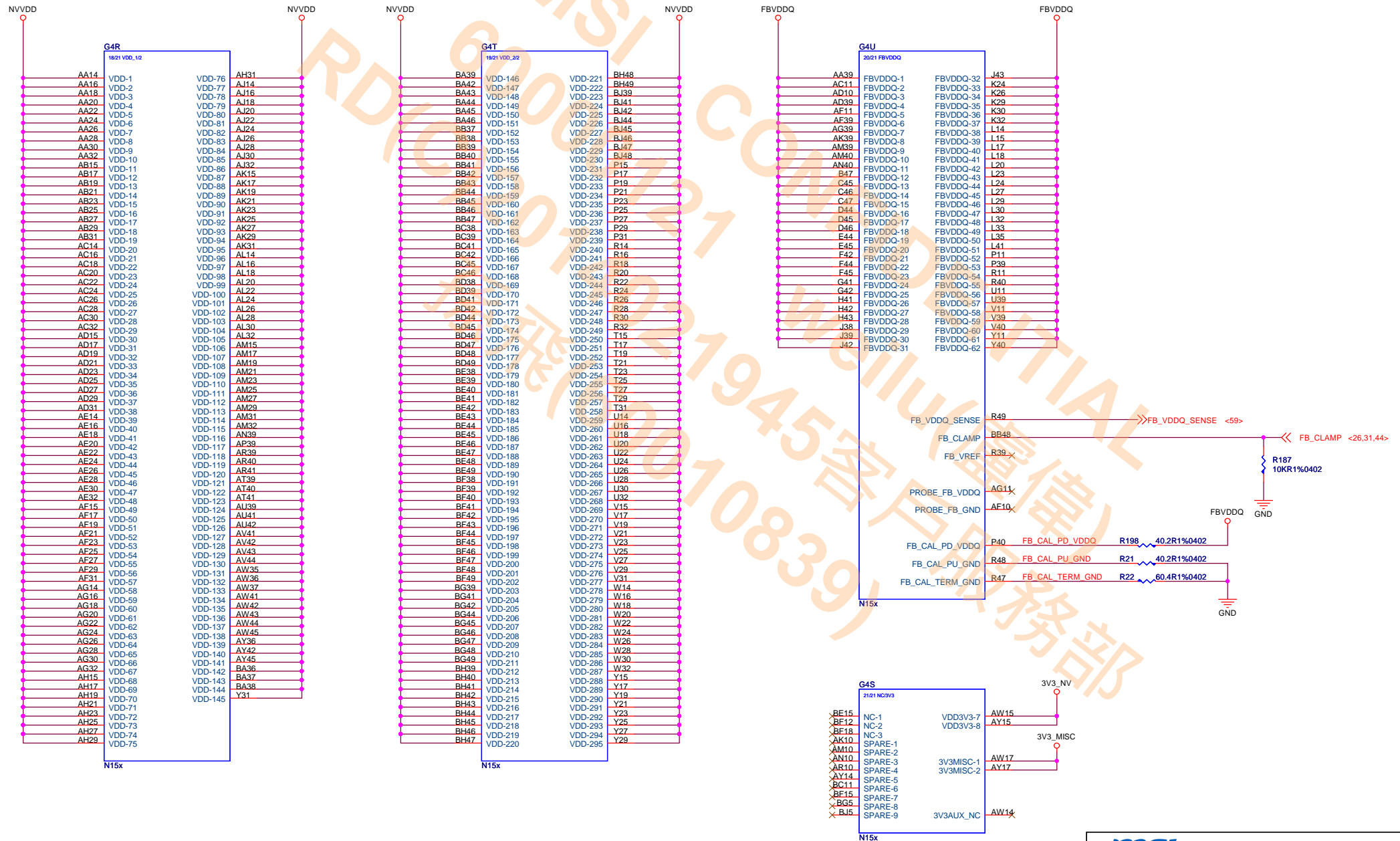
STRAP0	USER_BIT[3:0]	0xF: EDID	45K PU
STRAP1	3GIO_PADCFG_LUT_ADR[3:0]	0x0: DDI no used	5K PD
STRAP2	PCI_DEVID[3:0]	15E-GT 0x1199 15P-GX-B 0x119A	10K PU 15K PU
ROM_SO	VGA_DEVICE SMB_ALT_ADDR FB_0_BAR_SIZE XCLK_417	0x0001	5K PU
ROM_SI	RAM_CFG_0 RAM_CFG_1 RAM_CFG_2 RAM_CFG_3	0110 0111 0010 0001	35K PD 45K PD 15K PD 10K PD
ROM_SCLK	PCI_DEVID[4] SUB_VENDOR PCI_DEVID[5] PEX_PLL_EN_TERM100	1: 0x119=>1001 1: VBIOS ROM is Present 0: 0x119=>1001	25K PU
STRAP3	SOR_EXposed [3:0]	0000	5K PD
STRAP4	Reserved PCIE_Speed_Change_Gen3 PCIE_MAX_SPEED DP_PLL_VDD_33V	0 1: Enable PCIE Gen3 operation 1: Allow booting to GEN2/Gen3 1: ENABLED	45K PD

RGPU1 N15E-GT 5020 R11-0103T12-W08 X_10KR1%0402	R272 N15E-GT 10KR 1% N15P-GX-B 15KR 1%
DGPU1 5010 B03-0N15E05-N08 X_N15E-GT-A2	
RGPU2 N15P-GX-B 5020 R11-0153T12-W08 X_15KR1%0402	
DGPU2 5010 OB3-16H2001 X_N15P-GX-B-A2	





## GPU NVVDD, FBVDDQ



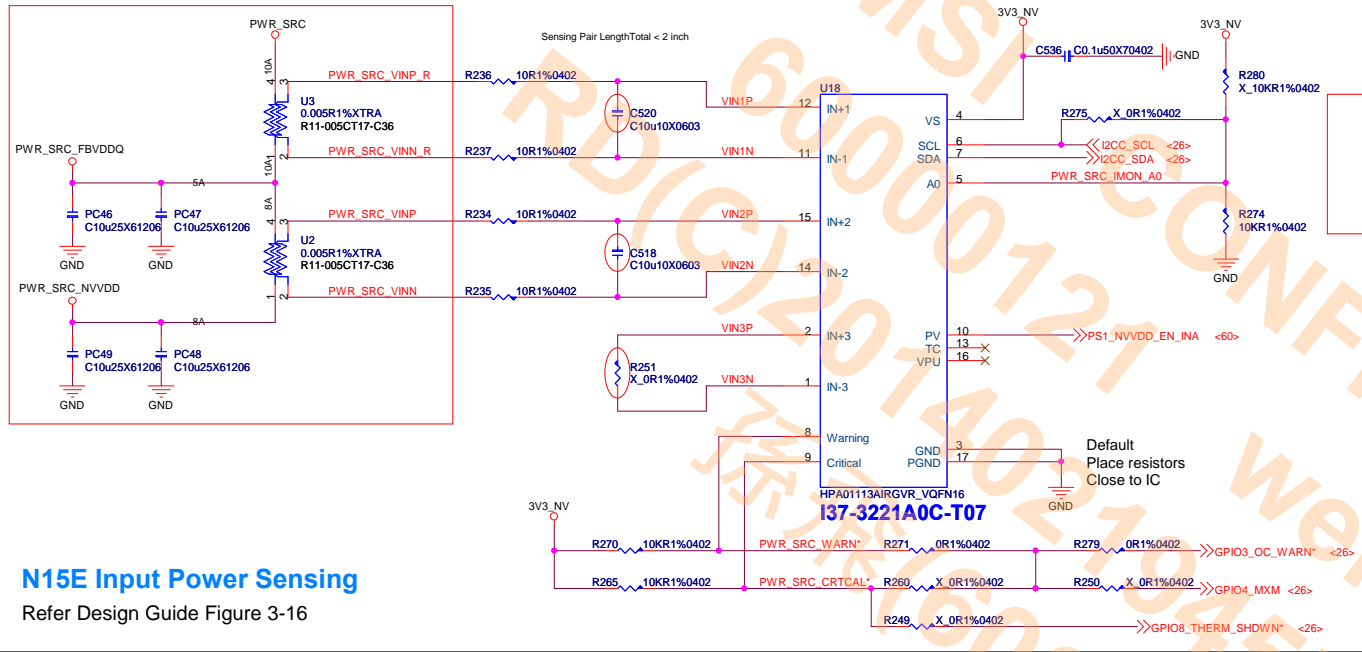
# DGPU GND

V61 GND_19		V72 GND_25	
A2	GND-1	BB32	GND-241
A3	GND-2	BB34	GND-242
A7	GND-3	BB36	GND-243
AA15	GND-4	BB38	GND-244
AA17	GND-5	BB39	GND-245
AA19	GND-6	BB40	GND-246
AA21	GND-7	BB41	GND-247
AA23	GND-8	BB42	GND-248
AA25	GND-9	BB43	GND-249
AA27	GND-10	BB44	GND-250
AA29	GND-11	BB45	GND-251
AA31	GND-12	BB46	GND-252
AA33	GND-13	BB47	GND-253
AA35	GND-14	BB48	GND-254
AA37	GND-15	BB49	GND-255
AA39	GND-16	BB50	GND-256
AA41	GND-17	BB51	GND-257
AA43	GND-18	BB52	GND-258
AA45	GND-19	BB53	GND-259
AA47	GND-20	BB54	GND-260
AA49	GND-21	BB55	GND-261
AA51	GND-22	BB56	GND-262
AA53	GND-23	BB57	GND-263
AA55	GND-24	BB58	GND-264
AA57	GND-25	BB59	GND-265
AA59	GND-26	BB60	GND-266
AA61	GND-27	BB61	GND-267
AA63	GND-28	BB62	GND-268
AA65	GND-29	BB63	GND-269
AA67	GND-30	BB64	GND-270
AA69	GND-31	BB65	GND-271
AA71	GND-32	BB66	GND-272
AA73	GND-33	BB67	GND-273
AA75	GND-34	BB68	GND-274
AA77	GND-35	BB69	GND-275
AA79	GND-36	BB70	GND-276
AA81	GND-37	BB71	GND-277
AA83	GND-38	BB72	GND-278
AA85	GND-39	BB73	GND-279
AA87	GND-40	BB74	GND-280
AA89	GND-41	BB75	GND-281
AA91	GND-42	BB76	GND-282
AA93	GND-43	BB77	GND-283
AA95	GND-44	BB78	GND-284
AA97	GND-45	BB79	GND-285
AA99	GND-46	BB80	GND-286
AB01	GND-47	BB81	GND-287
AB03	GND-48	BB82	GND-288
AB05	GND-49	BB83	GND-289
AB07	GND-50	BB84	GND-290
AB09	GND-51	BB85	GND-291
AB11	GND-52	BB86	GND-292
AB13	GND-53	BB87	GND-293
AB15	GND-54	BB88	GND-294
AB17	GND-55	BB89	GND-295
AB19	GND-56	BB90	GND-296
AB21	GND-57	BB91	GND-297
AB23	GND-58	BB92	GND-298
AB25	GND-59	BB93	GND-299
AB27	GND-60	BB94	GND-300
AB29	GND-61	BB95	GND-301
AB31	GND-62	BB96	GND-302
AB33	GND-63	BB97	GND-303
AB35	GND-64	BB98	GND-304
AB37	GND-65	BB99	GND-305
AB39	GND-66	BB00	GND-306
AB41	GND-67	BB01	GND-307
AB43	GND-68	BB02	GND-308
AB45	GND-69	BB03	GND-309
AB47	GND-70	BB04	GND-310
AB49	GND-71	BB05	GND-311
AB51	GND-72	BB06	GND-312
AB53	GND-73	BB07	GND-313
AB55	GND-74	BB08	GND-314
AB57	GND-75	BB09	GND-315
AB59	GND-76	BB10	GND-316
AB61	GND-77	BB11	GND-317
AB63	GND-78	BB12	GND-318
AB65	GND-79	BB13	GND-319
AB67	GND-80	BB14	GND-320
AB69	GND-81	BB15	GND-321
AB71	GND-82	BB16	GND-322
AB73	GND-83	BB17	GND-323
AB75	GND-84	BB18	GND-324
AB77	GND-85	BB19	GND-325
AB79	GND-86	BB20	GND-326
AB81	GND-87	BB21	GND-327
AB83	GND-88	BB22	GND-328
AB85	GND-89	BB23	GND-329
AB87	GND-90	BB24	GND-330
AB89	GND-91	BB25	GND-331
AB91	GND-92	BB26	GND-332
AB93	GND-93	BB27	GND-333
AB95	GND-94	BB28	GND-334
AB97	GND-95	BB29	GND-335
AB99	GND-96	BB30	GND-336
AB01	GND-97	BB31	GND-337
AB03	GND-98	BB32	GND-338
AB05	GND-99	BB33	GND-339
AB07	GND-100	BB34	GND-340
AB09	GND-101	BB35	GND-341
AB11	GND-102	BB36	GND-342
AB13	GND-103	BB37	GND-343
AB15	GND-104	BB38	GND-344
AB17	GND-105	BB39	GND-345
AB19	GND-106	BB40	GND-346
AB21	GND-107	BB41	GND-347
AB23	GND-108	BB42	GND-348
AB25	GND-109	BB43	GND-349
AB27	GND-110	BB44	GND-350
AB29	GND-111	BB45	GND-351
AB31	GND-112	BB46	GND-352
AB33	GND-113	BB47	GND-353
AB35	GND-114	BB48	GND-354
AB37	GND-115	BB49	GND-355
AB39	GND-116	BB50	GND-356
AB41	GND-117	BB51	GND-357
AB43	GND-118	BB52	GND-358
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AB63	GND-128	BB62	GND-368
AB65	GND-129	BB63	GND-369
AB67	GND-130	BB64	GND-370
AB69	GND-131	BB65	GND-371
AB71	GND-132	BB66	GND-372
AB73	GND-133	BB67	GND-373
AB75	GND-134	BB68	GND-374
AB77	GND-135	BB69	GND-375
AB79	GND-136	BB70	GND-376
AB81	GND-137	BB71	GND-377
AB83	GND-138	BB72	GND-378
AB85	GND-139	BB73	GND-379
AB87	GND-140	BB74	GND-380
AB89	GND-141	BB75	GND-381
AB91	GND-142	BB76	GND-382
AB93	GND-143	BB77	GND-383
AB95	GND-144	BB78	GND-384
AB97	GND-145	BB79	GND-385
AB99	GND-146	BB80	GND-386
AB01	GND-147	BB81	GND-387
AB03	GND-148	BB82	GND-388
AB05	GND-149	BB83	GND-389
AB07	GND-150	BB84	GND-390
AB09	GND-151	BB85	GND-391
AB11	GND-152	BB86	GND-392
AB13	GND-153	BB87	GND-393
AB15	GND-154	BB88	GND-394
AB17	GND-155	BB89	GND-395
AB19	GND-156	BB90	GND-396
AB21	GND-157	BB91	GND-397
AB23	GND-158	BB92	GND-398
AB25	GND-159	BB93	GND-399
AB27	GND-160	BB94	GND-400
AB29	GND-161	BB95	GND-401
AB31	GND-162	BB96	GND-402
AB33	GND-163	BB97	GND-403
AB35	GND-164	BB98	GND-404
AB37	GND-165	BB99	GND-405
AB39	GND-166	BB00	GND-406
AB41	GND-167	BB01	GND-407
AB43	GND-168	BB02	GND-408
AB45	GND-169	BB03	GND-409
AB47	GND-170	BB04	GND-410
AB49	GND-171	BB05	GND-411
AB51	GND-172	BB06	GND-412
AB53	GND-173	BB07	GND-413
AB55	GND-174	BB08	GND-414
AB57	GND-175	BB09	GND-415
AB59	GND-176	BB10	GND-416
AB61	GND-177	BB11	GND-417
AB63	GND-178	BB12	GND-418
AB65	GND-179	BB13	GND-419
AB67	GND-180	BB14	GND-420
AB69	GND-181	BB15	GND-421
AB71	GND-182	BB16	GND-422
AB73	GND-183	BB17	GND-423
AB75	GND-184	BB18	GND-424
AB77	GND-185	BB19	GND-425
AB79	GND-186	BB20	GND-426
AB81	GND-187	BB21	GND-427
AB83	GND-188	BB22	GND-428
AB85	GND-189	BB23	GND-429
AB87	GND-190	BB24	GND-430
AB89	GND-191	BB25	GND-431
AB91	GND-192	BB26	GND-432
AB93	GND-193	BB27	GND-433
AB95	GND-194	BB28	GND-434
AB97	GND-195	BB29	GND-435
AB99	GND-196	BB30	GND-436
AB01	GND-197	BB31	GND-437
AB03	GND-198	BB32	GND-438
AB05	GND-199	BB33	GND-439
AB07	GND-200	BB34	GND-440
AB09	GND-201	BB35	GND-441
AB11	GND-202	BB36	GND-442
AB13	GND-203	BB37	GND-443
AB15	GND-204	BB38	GND-444
AB17	GND-205	BB39	GND-445
AB19	GND-206	BB40	GND-446
AB21	GND-207	BB41	GND-447
AB23	GND-208	BB42	GND-448
AB25	GND-209	BB43	GND-449
AB27	GND-210	BB44	GND-450
AB29	GND-211	BB45	GND-451
AB31	GND-212	BB46	GND-452
AB33	GND-213	BB47	GND-453
AB35	GND-214	BB48	GND-454
AB37	GND-215	BB49	GND-455
AB39	GND-216	BB50	GND-456
AB41	GND-217	BB51	GND-457
AB43	GND-218	BB52	GND-458
AB45	GND-219	BB53	GND-459
AB47	GND-220	BB54	GND-460
AB49	GND-221	BB55	GND-461
AB51	GND-222	BB56	GND-462
AB53	GND-223	BB57	GND-463
AB55	GND-224	BB58	GND-464
AB57	GND-225	BB59	GND-465
AB59	GND-226	BB60	GND-466
AB61	GND-227	BB61	GND-467
AB63	GND-228	BB62	GND-468
AB65	GND-229	BB63	GND-469
AB67	GND-230	BB64	GND-470
AB69	GND-231	BB65	GND-471
AB71	GND-232	BB66	GND-472
AB73	GND-233	BB67	GND-473
AB75	GND-234	BB68	GND-474
AB77	GND-235	BB69	GND-475
AB79	GND-236	BB70	GND-476
AB81	GND-237	BB71	GND-477
AB83	GND-238	BB72	GND-478
AB85	GND-239	BB73	GND-479
AB87	GND-240	BB74	GND-480
AB89	GND-241	BB75	GND-481
AB91	GND-242	BB76	GND-482

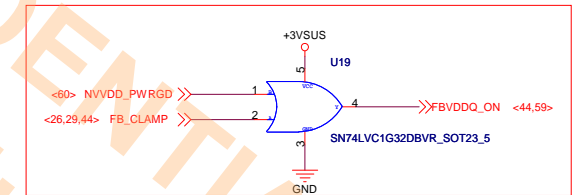
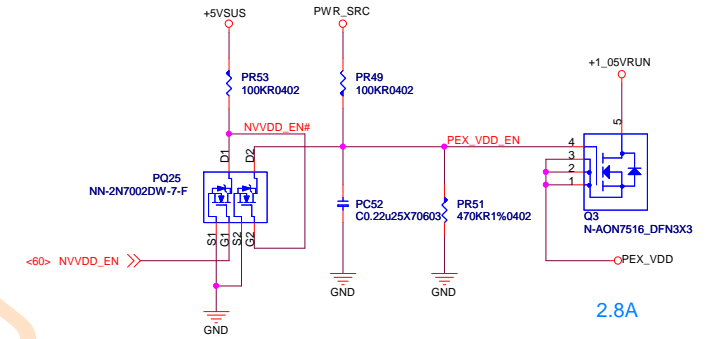
G4Q  
N15x

G4P  
N15x

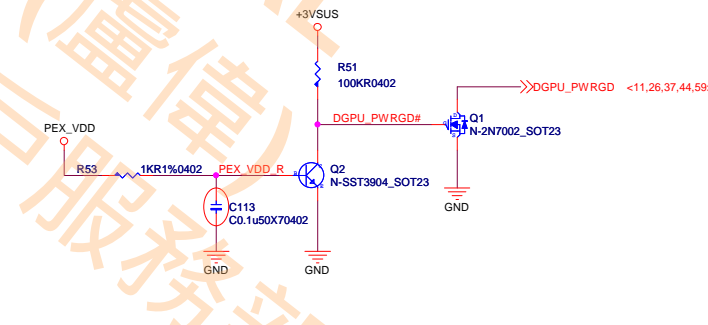
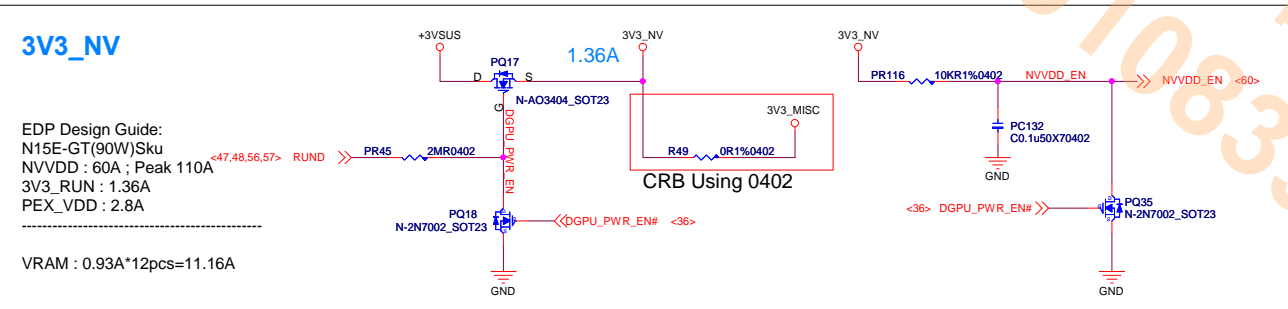
# DGPU\_Power Control



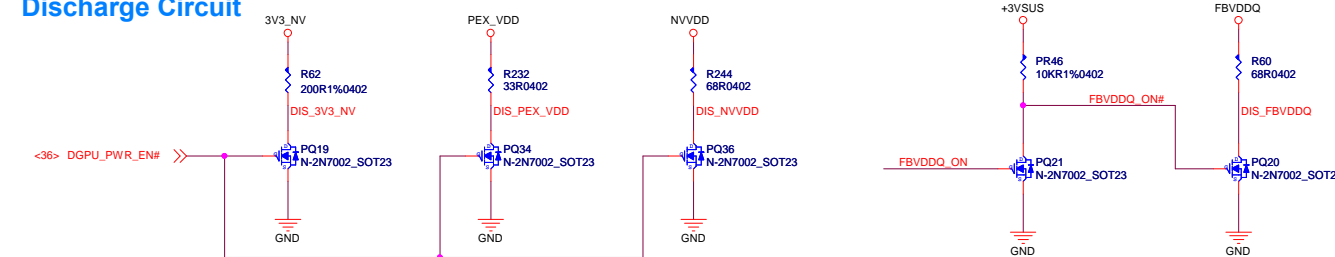
## PEX\_VDD



## nVIDIA Power Sequence Control 3V3\_NV -> NVVDD, PEX\_VDD -> FBVDDQ -> DGPUPWRGD

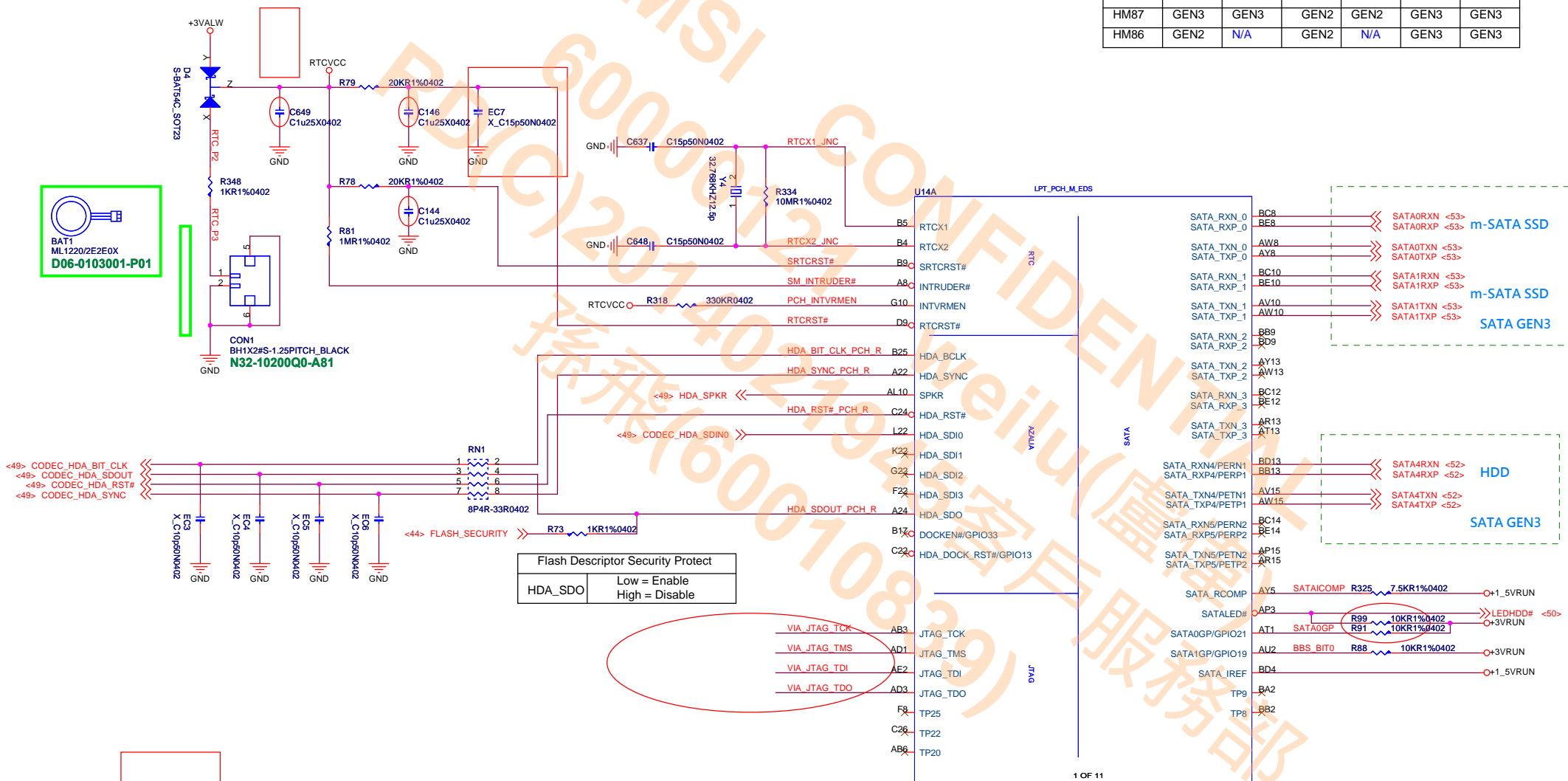


## Discharge Circuit



# Lynx Point ( HDA/JTAG/SATA )

SKU	High Speed SATA I/O Ports					
	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5
HM87	GEN3	GEN3	GEN2	GEN2	GEN3	GEN3
HM86	GEN2	N/A	GEN2	N/A	GEN3	GEN3




SPK The Signal has a weak internal pull-down  
Note: the internal pull-down is disabled after PLTRST# deasserts.  
If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode  
(Panther Point will disable the TCO Timer system reboot feature)

## Lynx Point (Clock)

PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH. Intel recommends terminating PCIECLKREQ# pin on PCH with 10 k $\Omega$   $\pm$ 10% external pull-up resistor instead of No Connect. Only PCIECLKREQ[2:1]# on PCH are core well powered. All other PCIECLKREQ# are suspend well powered.

2 OF 11

		<b>MICRO-STAR INT'L CO.,LTD.</b>	
<b>Title</b>			
<b>PCH-2 ( CLK )</b>			
<b>Size</b>	<b>Document Number</b>		<b>Rev</b>
<b>MS-16H2</b>		<b>0A</b>	
<b>Date:</b>	<b>Thursday, September 05, 2013</b>	<b>Sheet</b>	<b>33 of 71</b>



U14D LPT\_PCH\_M\_EDS

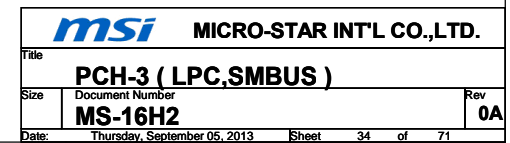
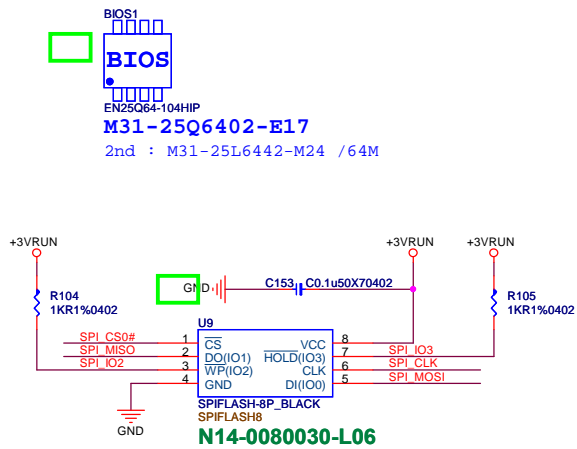
Signal	Internal Label	External Label	Notes
LAD_0	SMBus	SMBALERT#/GPIO11	N7
LAD_1		SMBCLK	R10
LAD_2		SMBDATA	U11
LAD_3		SML0ALERT#/GPIO60	N8
LFRAME#	SML0	SML0CLK	U8
LDRQ0#		SML0DATA	R7
LDRQ1#/GPIO23		SML1ALERT#/PCHHOT#/GPIO74	H6
SERIRQ		SML1CLK/GPIO58	K6
SPI_CLK	C-Link	SML1DATA/GPIO75	N11
SPI_CS0#		CL_CLK	AF11
SPI_CS1#		CL_DATA	AF10
SPI_CS2#		CL_RST#	AF7
SPI_MOSI	Thermal	TP1	BA45
SPI_MISO		TP2	BC45
SPI_IO2		TP4	BE43
SPI_IO3		TP3	BE44
		TD_IREF	AY43
			R70 8.2K R1%0402
			GND

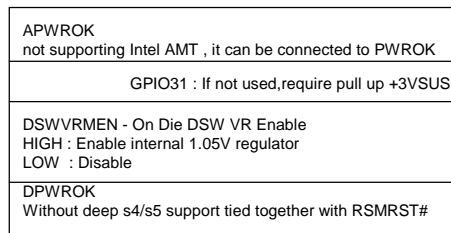
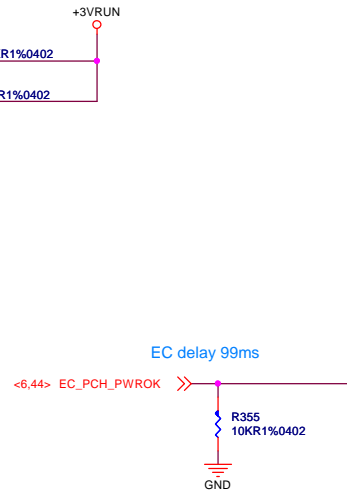
3 OF 11

Notes:

- SMBALERT#/GPIO11 << SCI\_WAKE\_UP# <44>
- SUS\_SMBCLK
- SUS\_SMBDATA
- DRAMRST\_CNTRL\_PCH
- SML0\_CLK
- SML0\_DATA
- PCH\_GPIO74
- SML1\_CLK
- SML1\_DATA
- SML1不使用PCH 温度
- PCH\_GPIO74
- SCI\_WAKE\_UP#
- DRAMRST\_CNTRL
- SML0\_CLK
- SML0\_DATA
- SML1\_DATA
- SML1\_CLK

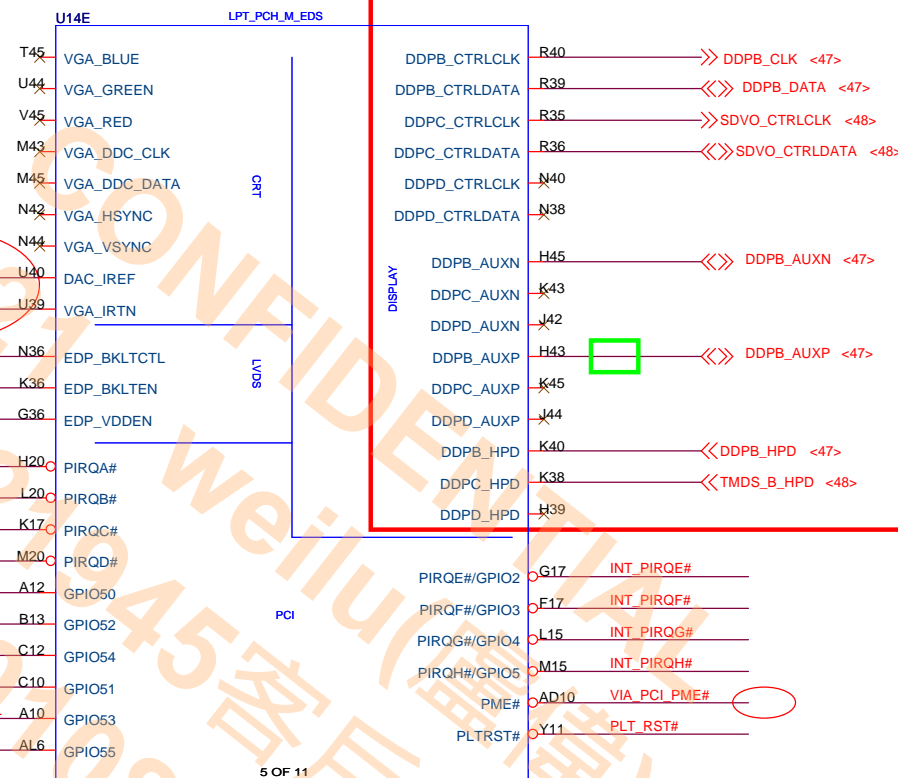
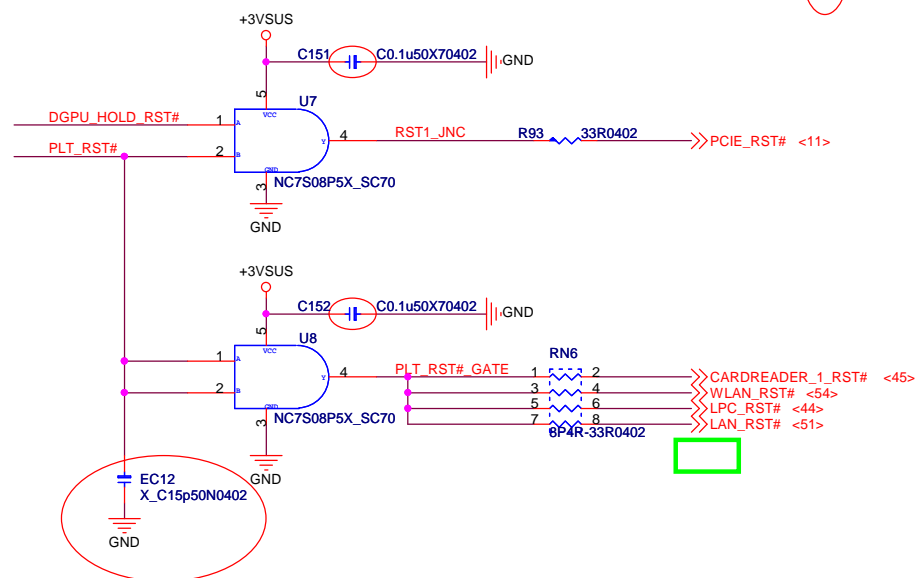
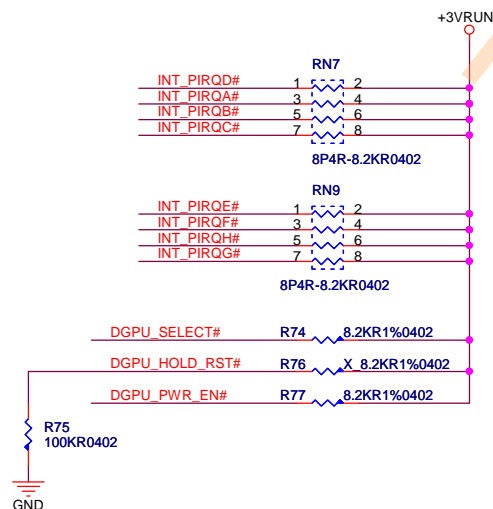
+3VRUN





PLL ON DIE VR_ENABLE	
GPIO62	Internal pull high (Enable)
	Low: Disable

## Lynx Point ( PCI,DDI )



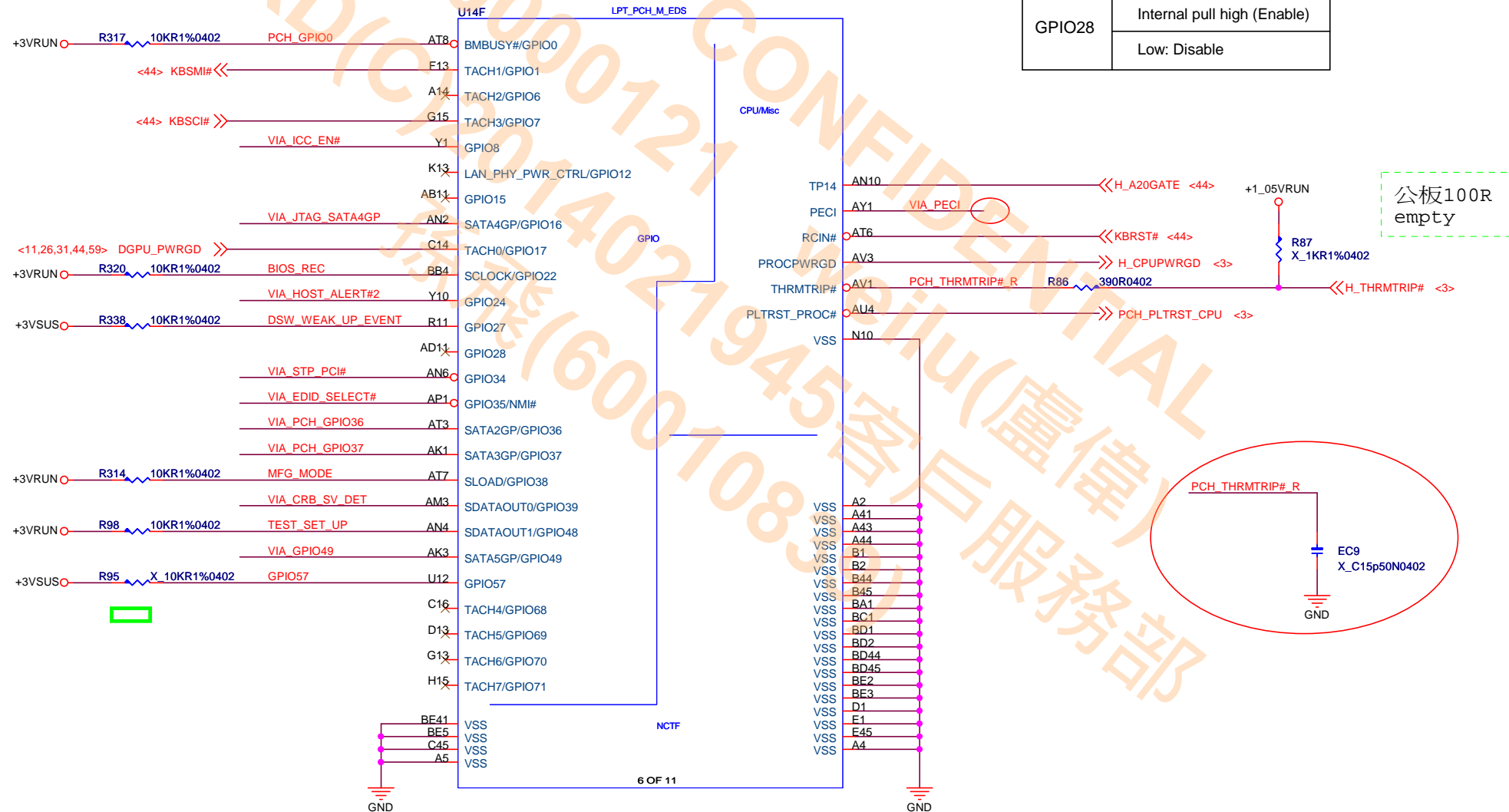
DDI-B : DP  
DDI-C : HDMI

Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	N/A
1	1	SPI

# Lynx Point ( GPIO,MISC )

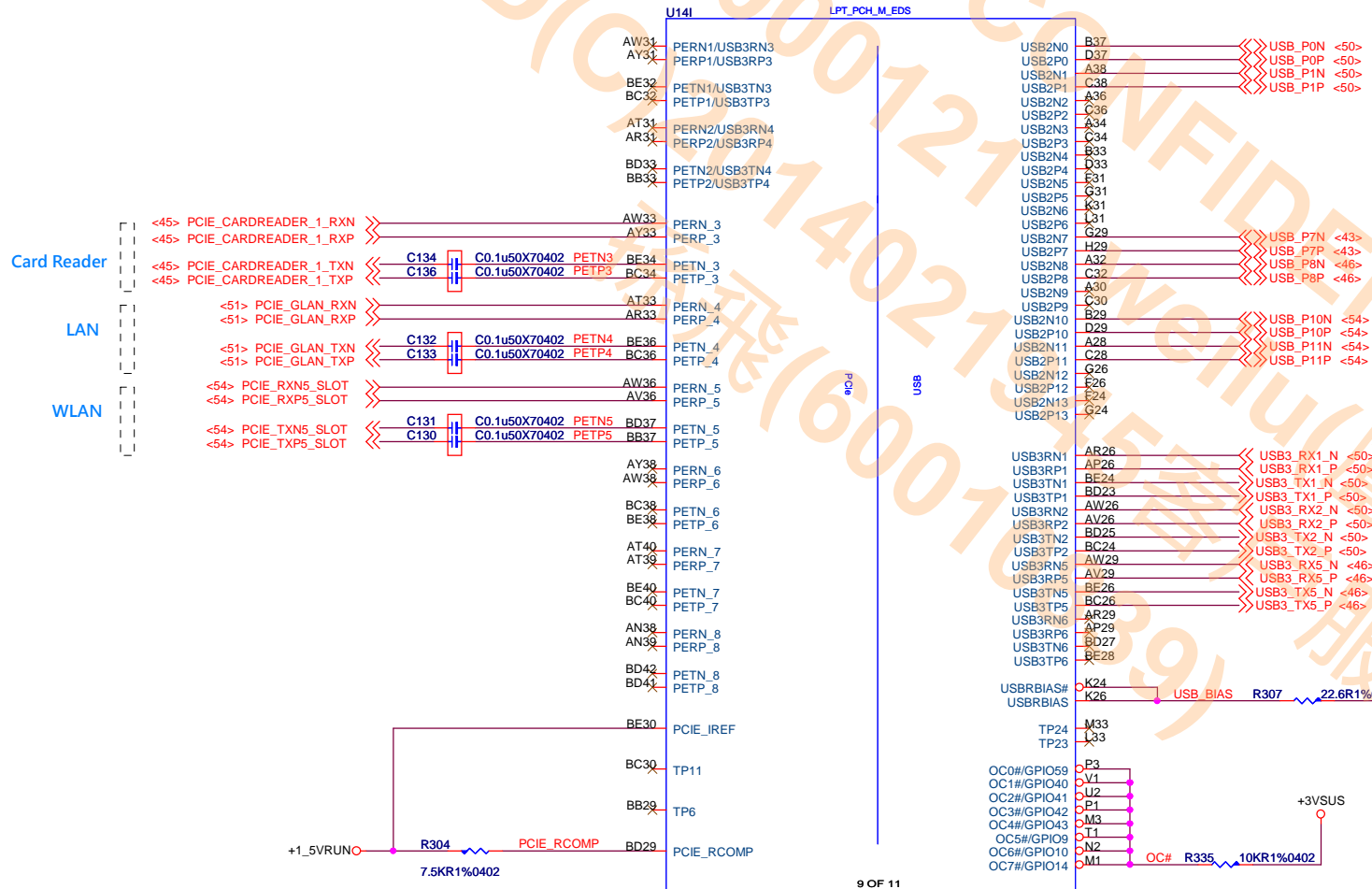
GPIO Setting : Ref 486708\_LPT\_EDS Section2.24

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable



# Lynx Point ( PCIE,USB )

Intel Lynx Point ECHI USB(2.0) debug transport 需接Port1 or Port9



USB			
USB 2.0	USB 3.0	Device	Note
0	1	USB 3.0 Port 1	16H2A
1	2	USB 3.0 Port 2	16H2A
2			NC
3			NC
4			NC
5			NC
6			NC
7		EPF021	3 色KBC
8	3	USB 3.0 Port 5	16H21
9			NC
10		WLAN	
11		WebCam	
12		SECOND DISPLAY	
13			NC

HM86 没USB3.0 PORT 5,6

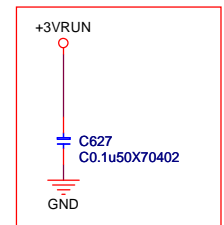
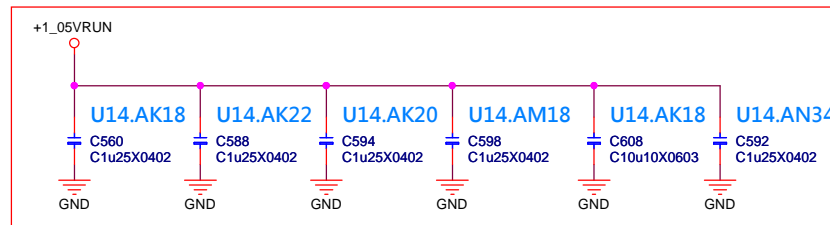
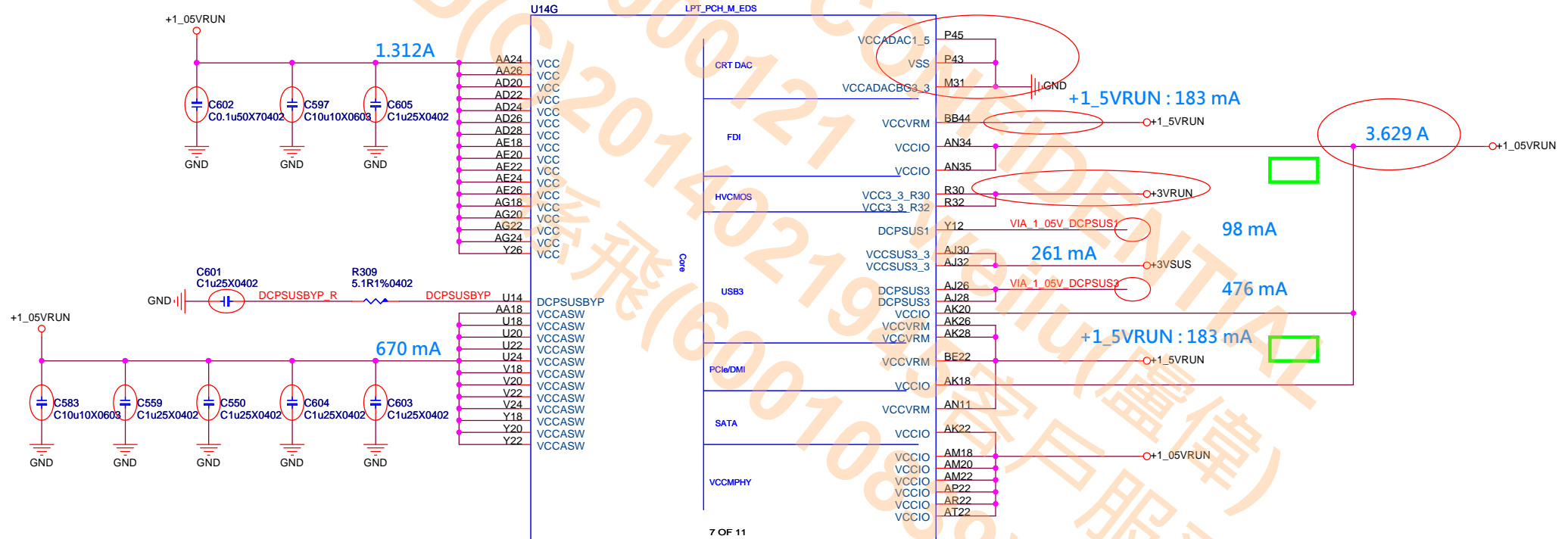


MICRO-STAR INT'L CO.,LTD.

Title <b>PCH-7 ( PCIE,USB )</b>		
Size	Document Number <b>MS-16H2</b>	Rev <b>0A</b>
Date:	Thursday, September 05, 2013	Sheet 38 of 71



# Lynx Point ( Power )



msi

MICRO-STAR INT'L CO.,LTD.

Title PCH-8 ( Power )

Size Document Number MS-16H2 Rev 0A

Date: Thursday, September 05, 2013 Sheet 39 of 71

**Power supply diagram for the Lynx (Power) board.**

**Legend:**

- USB:** VCCSUS3\_3, VCCDSW3\_3, DCPSSST, VCC3\_3, VCC3\_3, VCC3\_3, VCCIO
- Azalia:** VCCSUSHDA
- RTC:** VCCRTC, DCPRTC, DCPRTC
- CPU:** V\_PROC\_IO, V\_PROC\_IO
- SPI:** VCCSPI
- Thermal:** VCCVRM, VCC3\_3, VCC3\_3

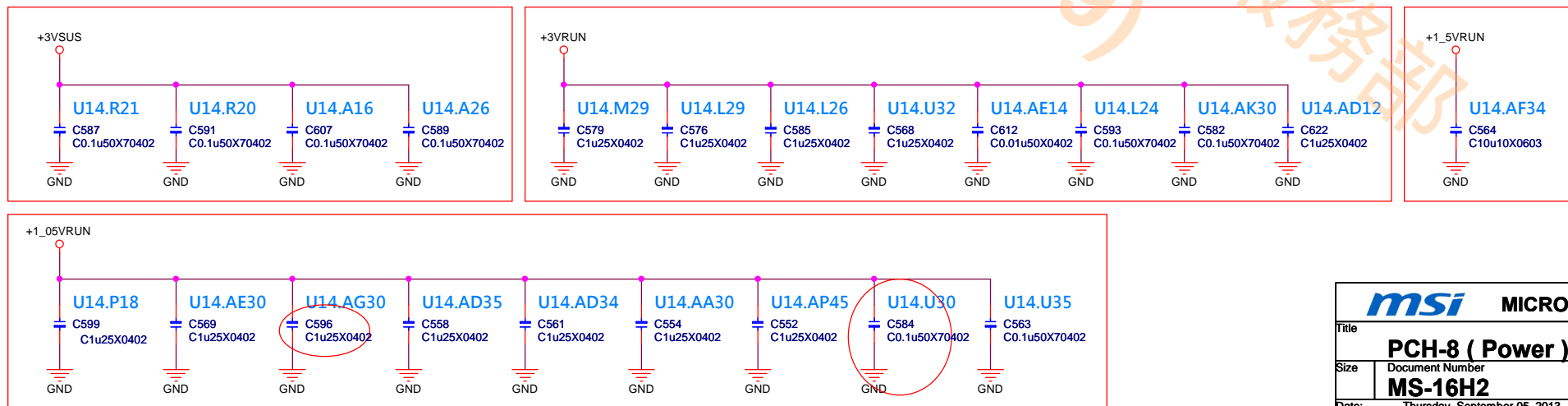
**Power Rails and Currents:**

- +3VSUS:** 261 mA (R20, R22)
- +3V3:** 15 mA (A16)
- +3V3RUN:** 133 mA (AE14, AF12, AG14)
- +1\_05VRUN:** 10 mA (A26)
- +3V3:** 261 mA (K8)
- +3V3 K8:** 261 mA (K8)
- +1\_05V\_AJ12:** 4 mA (AJ12, AJ14)
- +3V3RUN:** 22 mA (AD12)
- +1\_05VRUN:** 670 mA (P18, P20, L17, R18)
- +1\_05VRUN:** (AW40)
- +3V3RUN:** (AK30, AK32)

**Other Components:**

- RTCVCC:** (A6)
- 1\_05V\_AJ12:** (AJ12, AJ14)
- R313:** (R313)
- OR1%0402:** (OR1%0402)
- 1\_05V\_RUN:** (1\_05V\_RUN)

**8 OF 11**

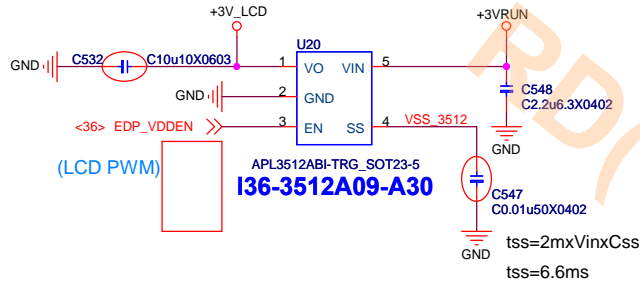


# Lynx Point ( GND )

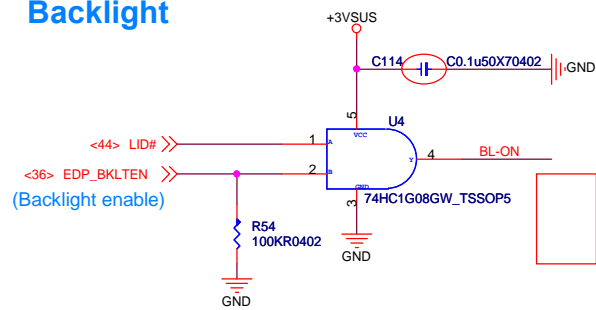


# eDP Connector

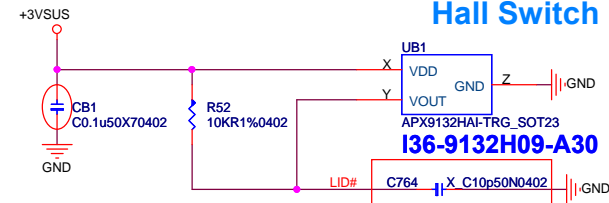
## Pannel Device Logic Power



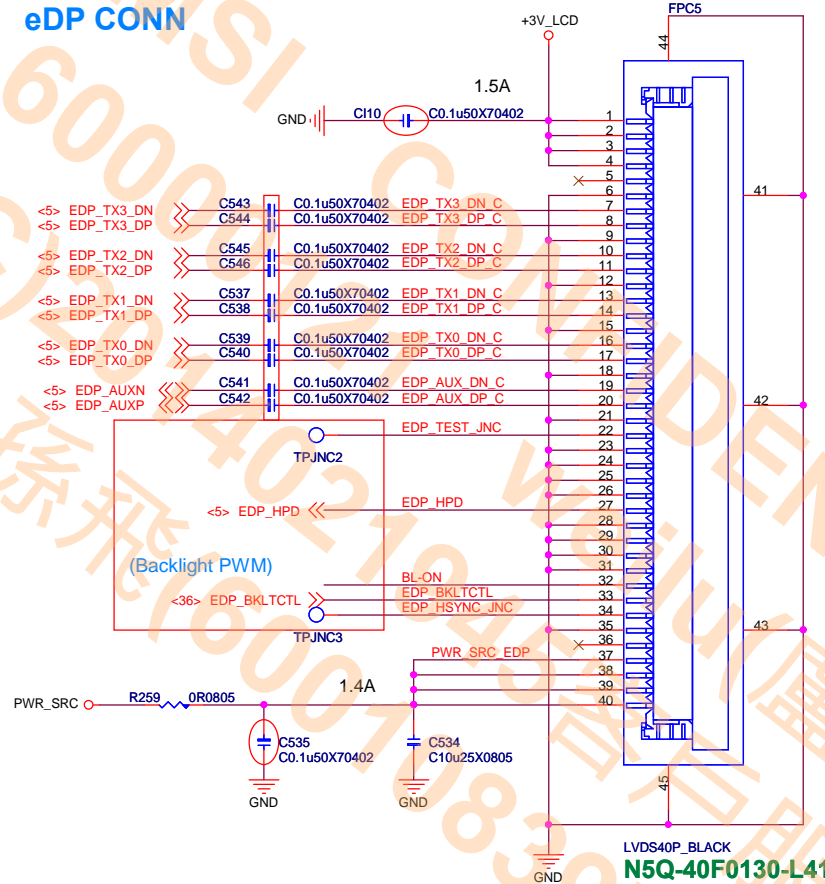
## Backlight



## Hall Switch



## eDP CONN

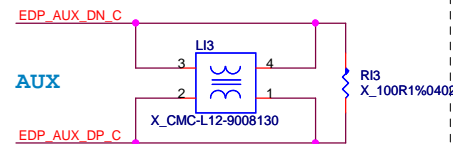
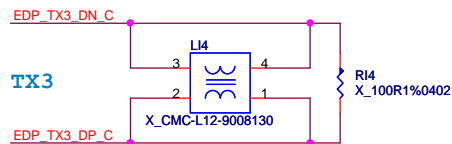
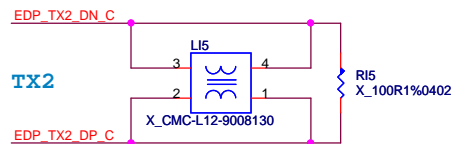
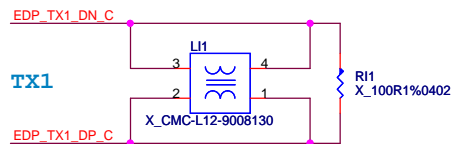
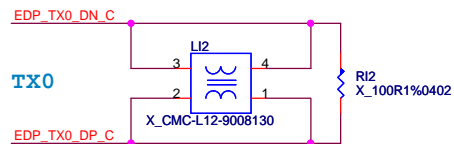


## LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPDP	HPDP signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

Place Close eDP Connector

Reserve for EMI

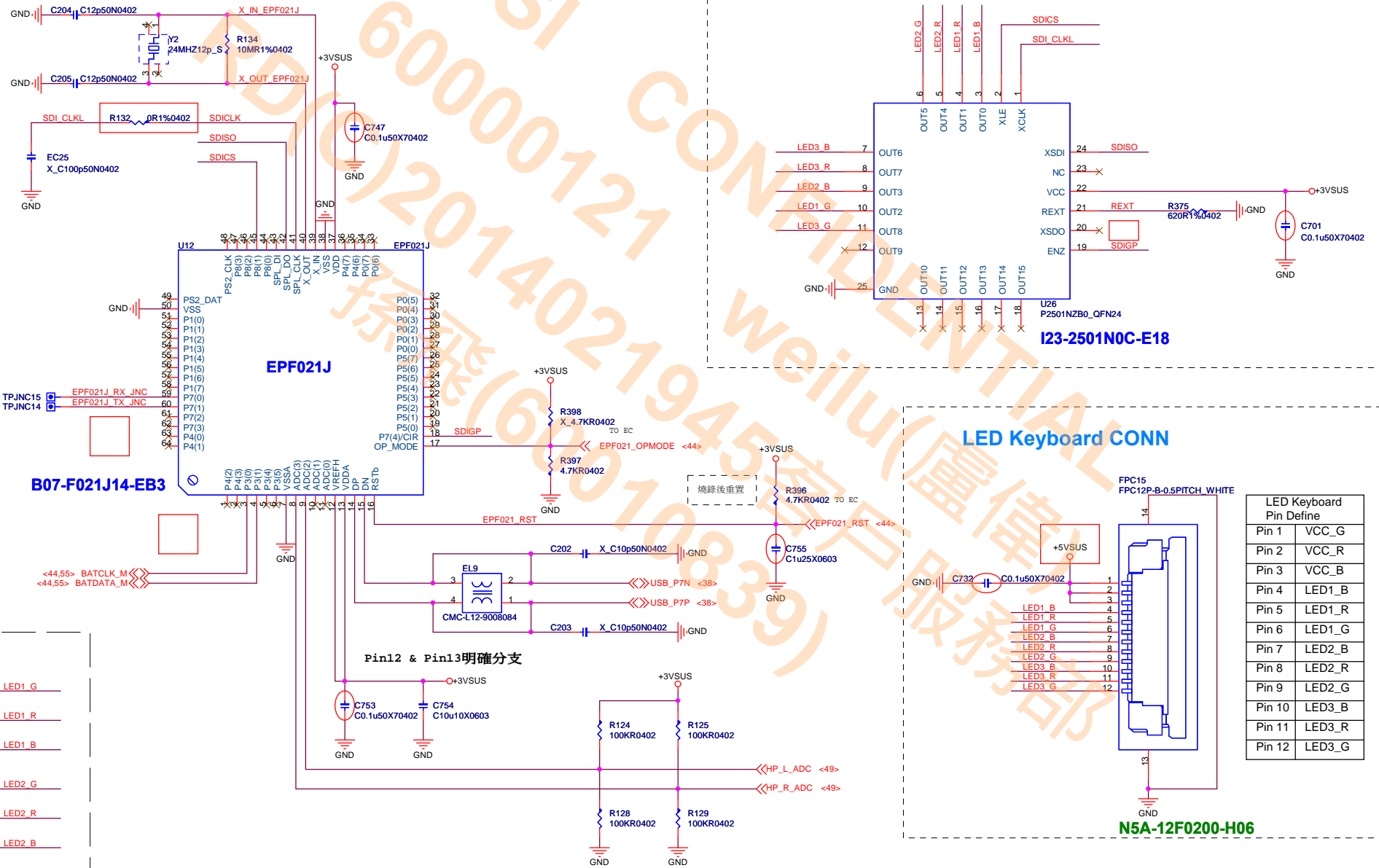


msi

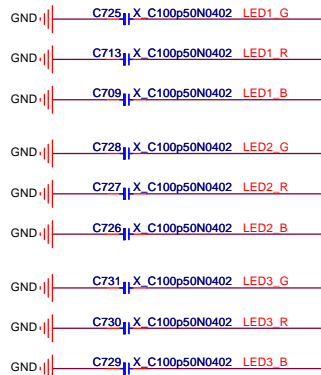
MICRO-STAR INT'L CO.,LTD.

Title		eDP Connector	
Size	Document Number	MS-16H2	
Date:	Thursday, September 05, 2013	Sheet	42 of 71
Rev		0A	

# LED 8051 Controller



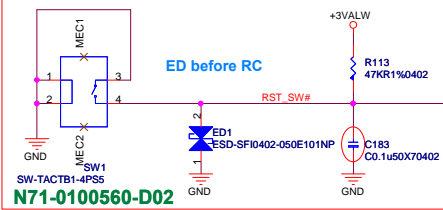
## EMI



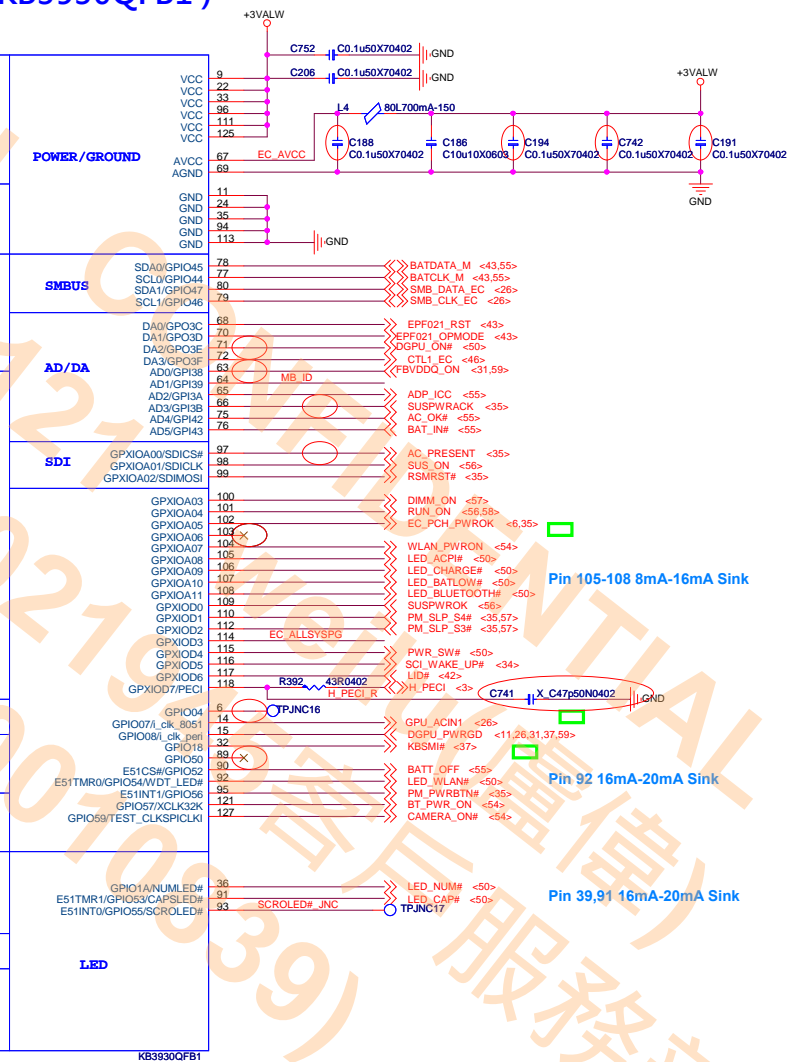
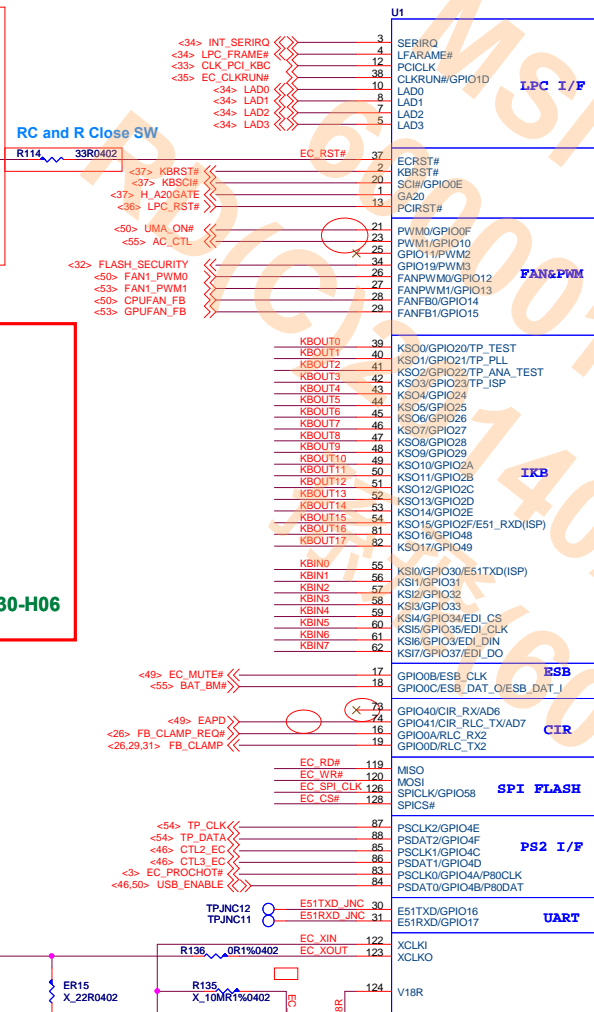
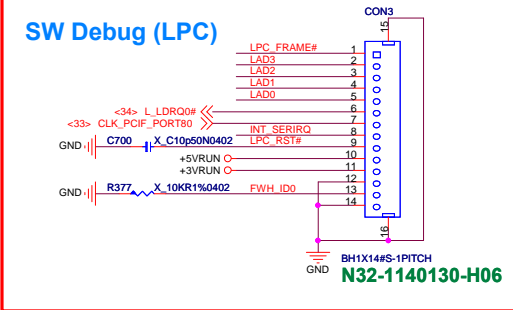


KBC( KB3930QFB1 )

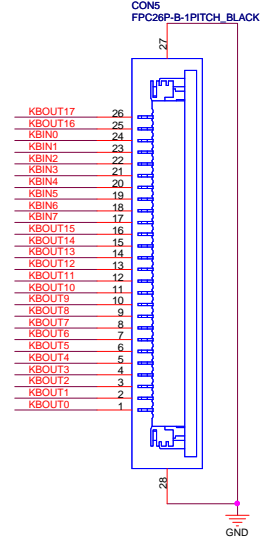
## Hardware Reset



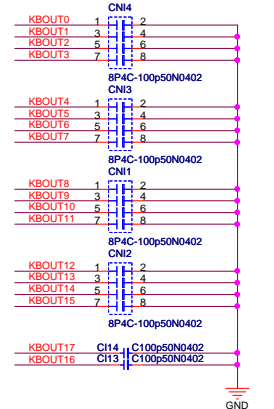
## SW Debug (LPC)



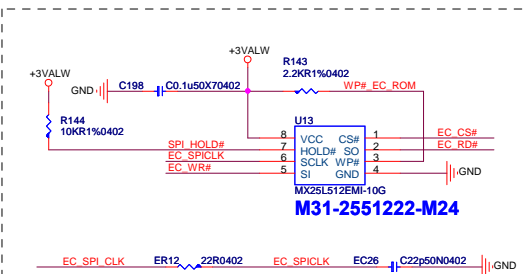
## Keyboard conn



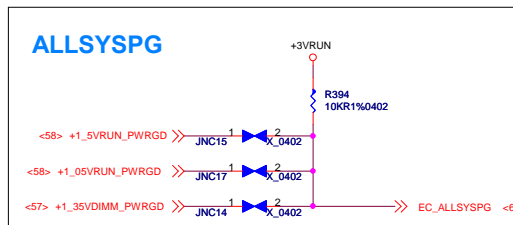
**N5A-26F0340-H06**



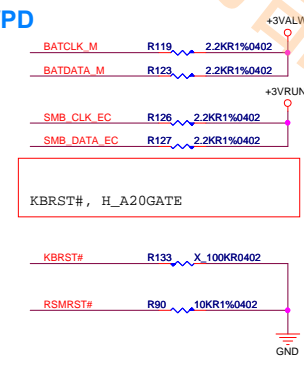
## ROM



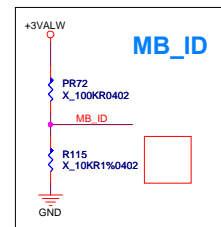
**ALLSYSPG**



PU/PD



## MB\_ID

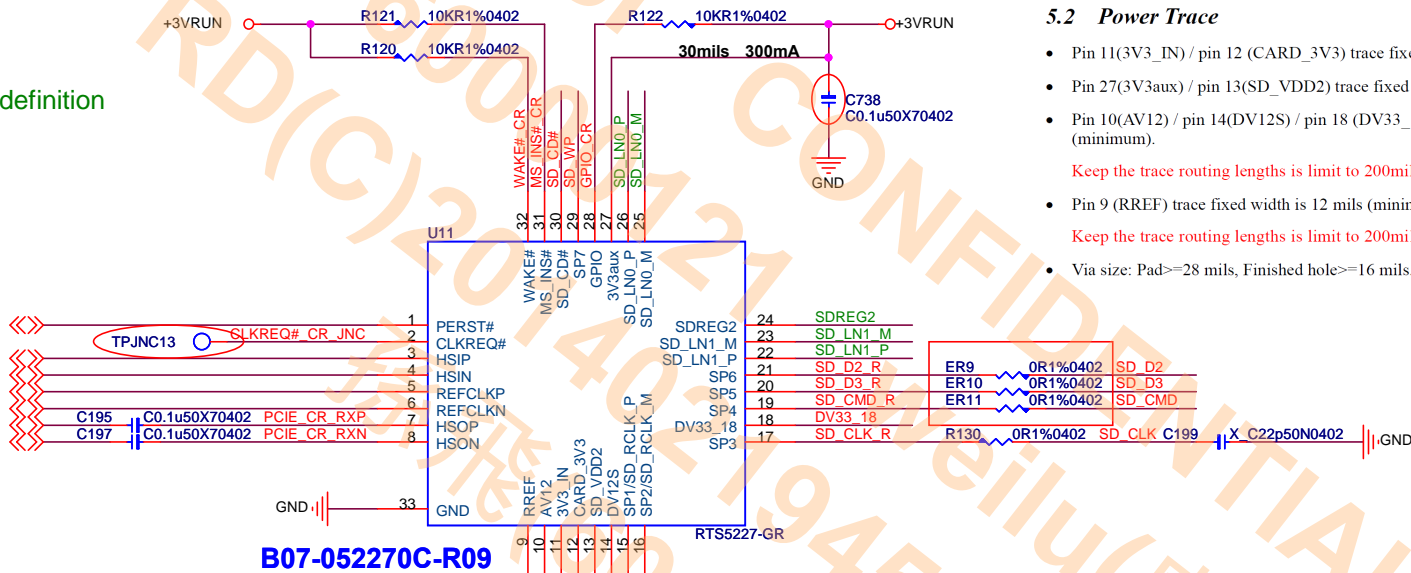


# CardReader ( RTS5227 )

RTS5249 Colay RTS5227

Pin 13/15/16/22/23/24/25/26 definition are different from RTS5227

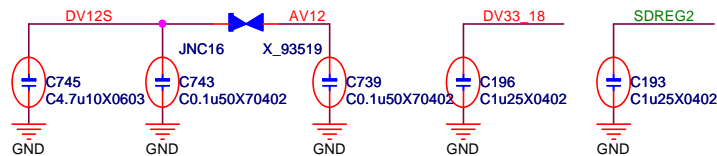
<36> CARDREADER\_1\_RST#  
<38> PCIE\_CARDREADER\_1\_TXP  
<38> PCIE\_CARDREADER\_1\_TXN  
<33> CLK\_CARDREADER\_1\_P  
<33> CLK\_CARDREADER\_1\_N  
<38> PCIE\_CARDREADER\_1\_RXP  
<38> PCIE\_CARDREADER\_1\_RXN



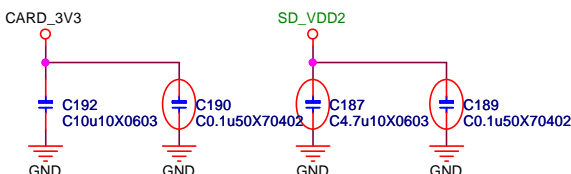
## 5.2 Power Trace

- Pin 11(3V3\_IN) / pin 12 (CARD\_3V3) trace fixed width is 40 mils (minimum).
- Pin 27(3V3aux) / pin 13(SD\_VDD2) trace fixed width is 30 mils (minimum).
- Pin 10(AV12) / pin 14(DV12S) / pin 18 (DV33\_18) / pin 24(SDREG2) trace fixed width is 20 mils (minimum).
- Keep the trace routing lengths is limit to 200mils.
- Pin 9 (RREF) trace fixed width is 12 mils (minimum).
- Keep the trace routing lengths is limit to 200mils.
- Via size: Pad>=28 mils, Finished hole>=16 mils.

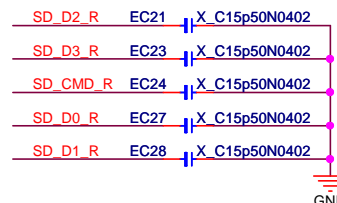
## Close Chip



## Close Connector

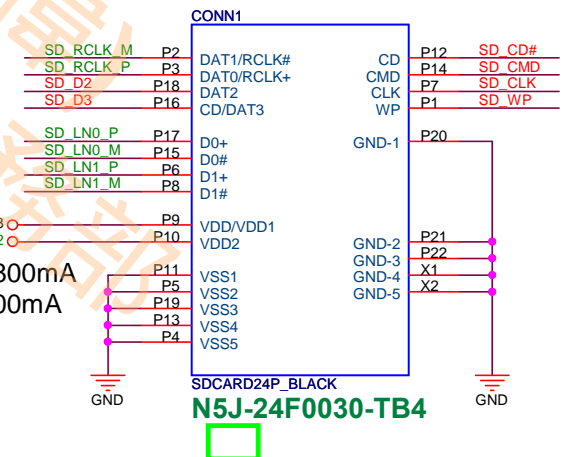


## EMI



SD3.0 1.8V  
SD4.0 1.2V

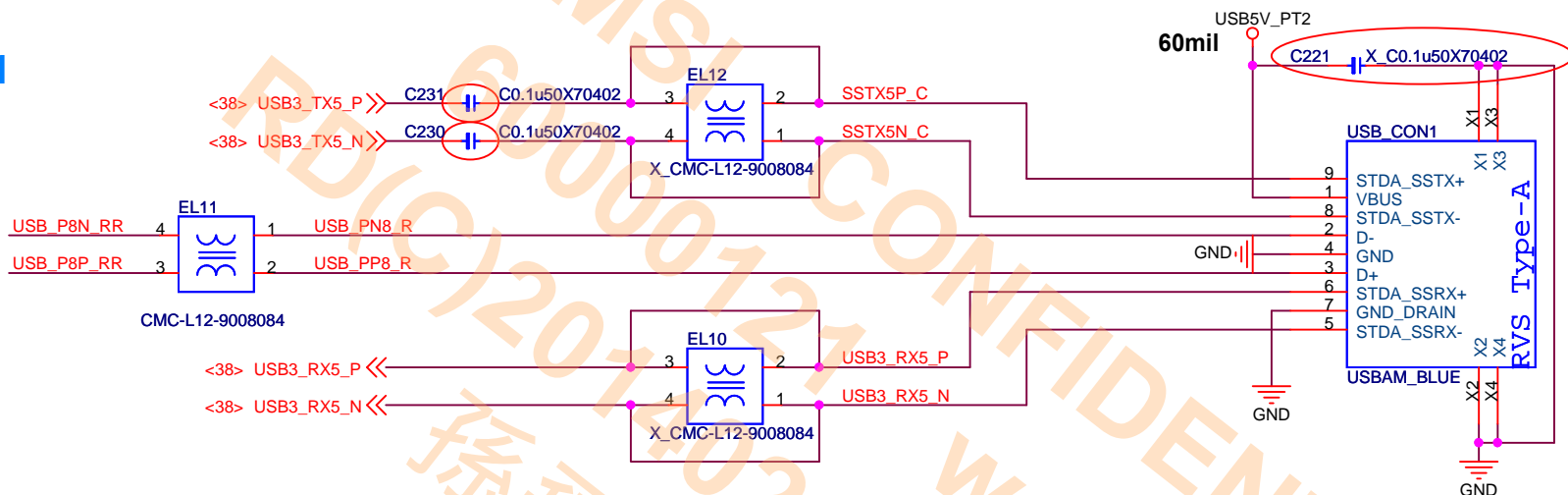
CARD\_3V3: 800mA  
SD\_VDD2: 200mA



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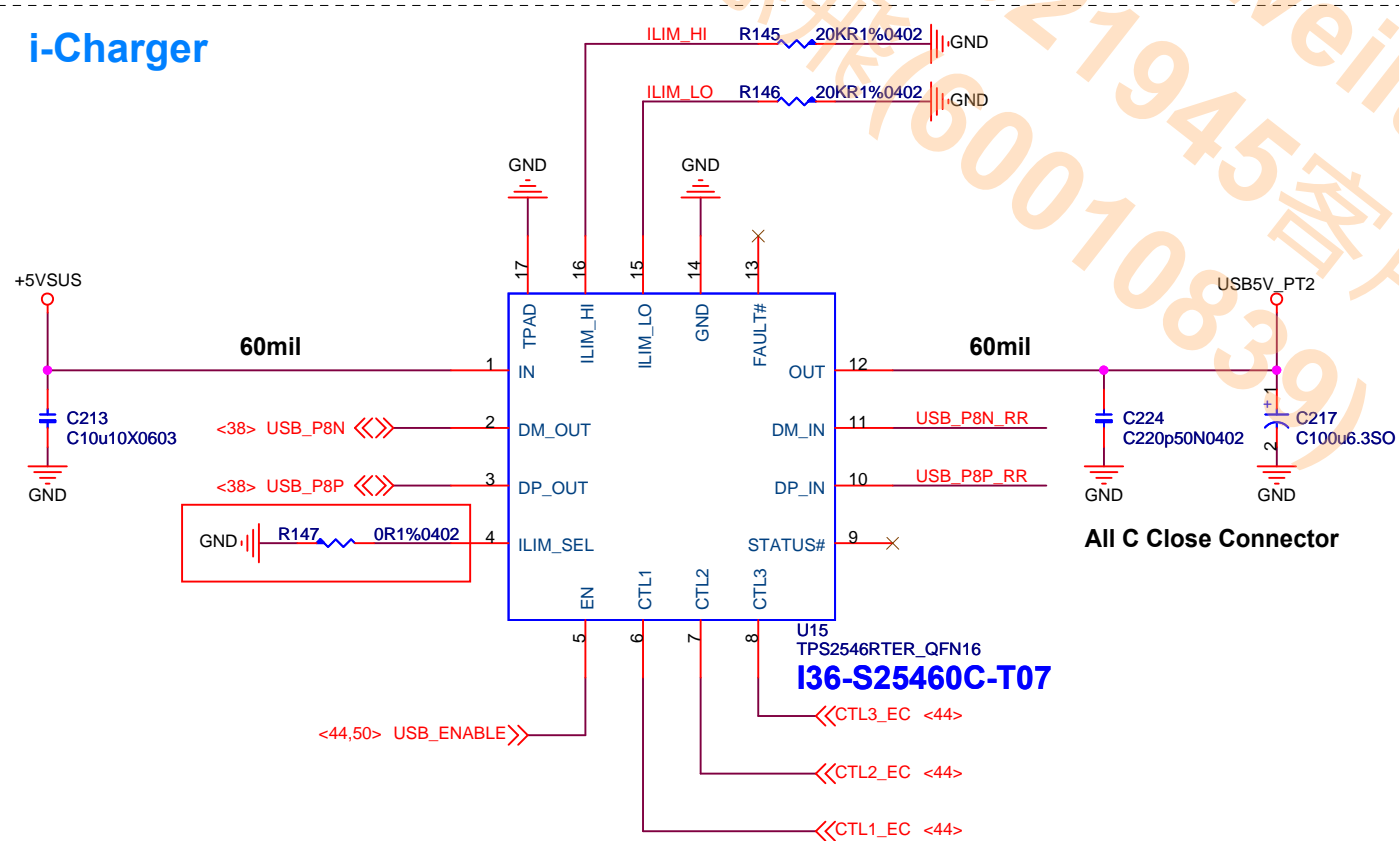
Title			Card Reader/USB3.0 CNT-1/-2
Size	Document Number		MS-16H2
Date:	Thursday, September 05, 2013	Sheet	45 of 71
Rev	0A		

**USB3.0 Port-6**  
**USB2.0 Port-9**

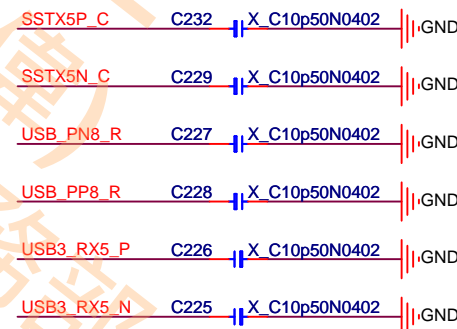


**N53-09M0241-AF2**

## i-Charger

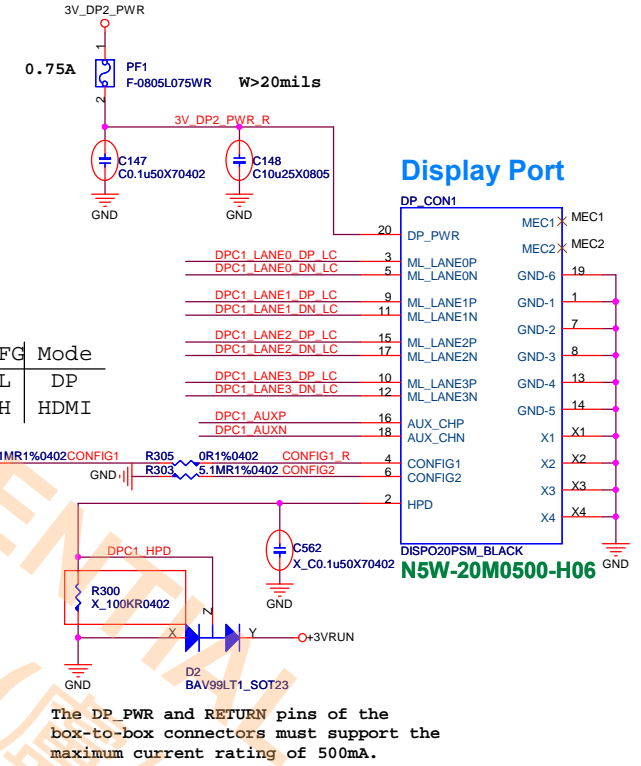
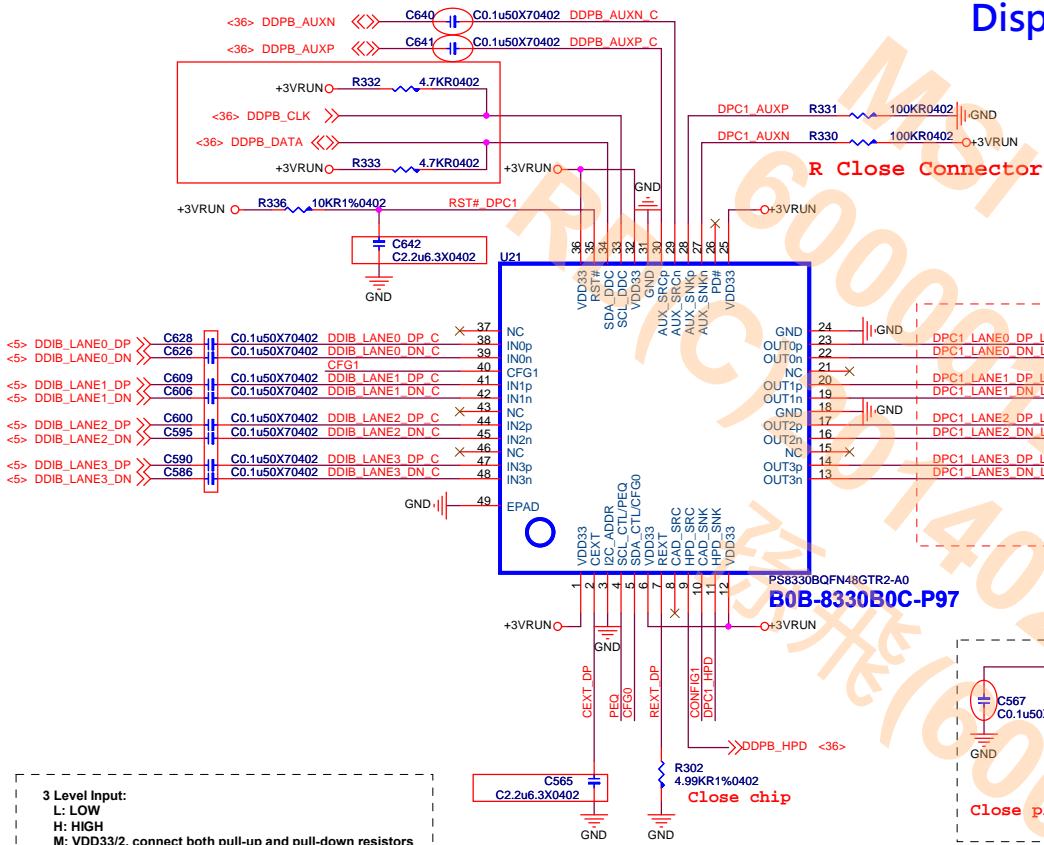


## EMI



## All C Close Connector

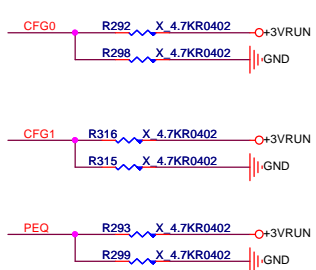
## Display Port



The DP\_PWR and RETURN pins of the box-to-box connectors must support the maximum current rating of 500mA.

HPD\_SNK Have internal Pull down 150kohm.  
No problem with Leakage from DP device

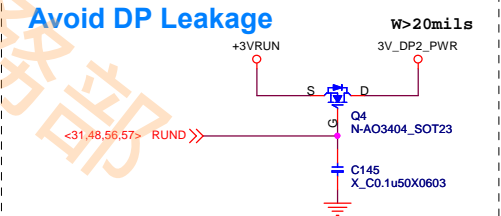
CAD\_SNK Have internal Pull down 1Mohm.



```
Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k Ohm, 3.3V I/O.
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing
```

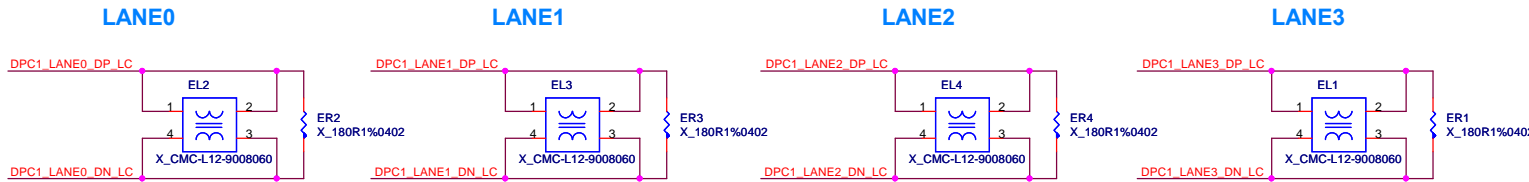
```
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K Ohm
H: default, auto test disable & input offset cancellation enable
L: auto test enable & input offset cancellation enable
M: auto test disable & input offset cancellation disable
```

Programmable input equalization levels; Internal pull down at ~150k Ohm, 3.3V I/O.  
 L: default, LEQ, compensate channel loss up to 12dB @ HBR2  
 H: HEQ, compensate channel loss up to 15dB @ HBR2  
 M: LLEQ, compensate channel loss up to 5dB @ HBR2

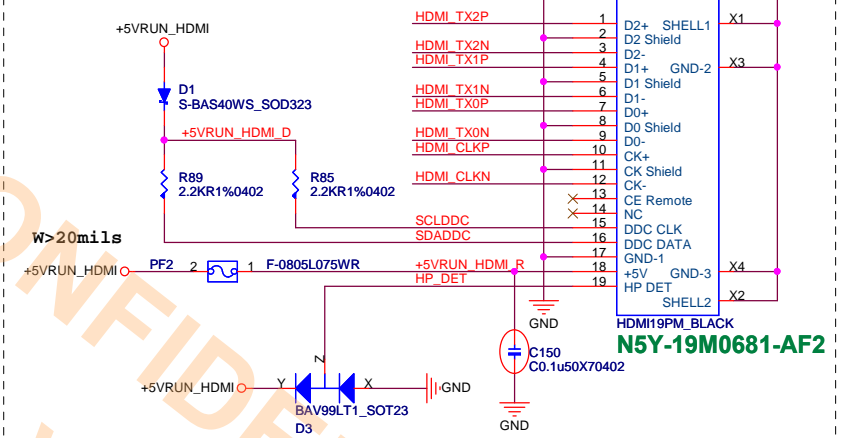
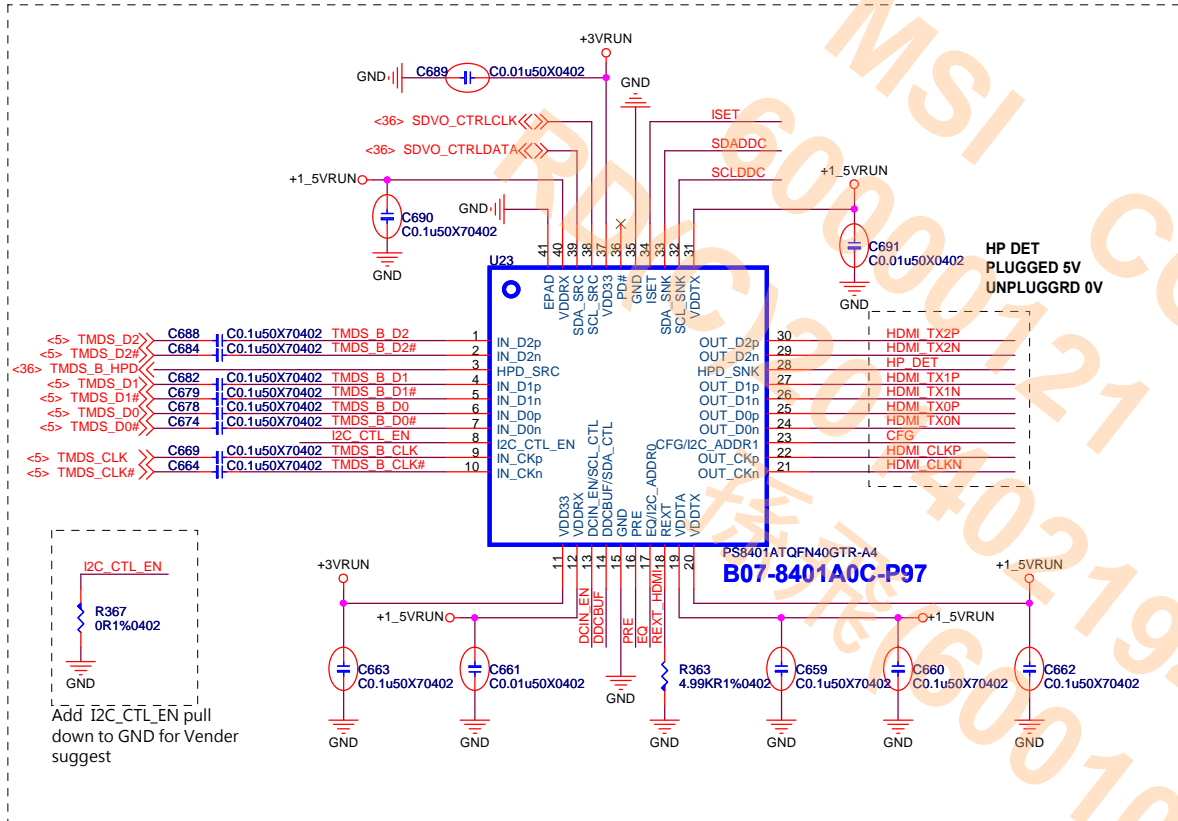


## EMI Close Connector

### LANE0

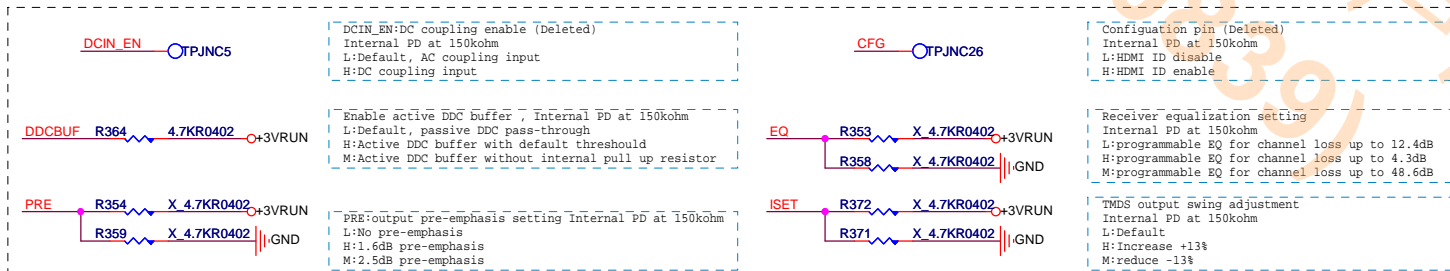


## HDMI Repeater

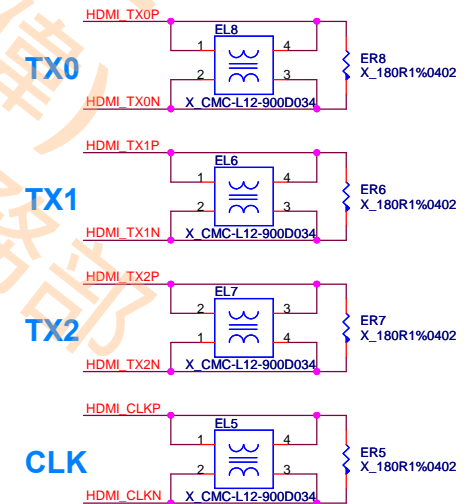


An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.

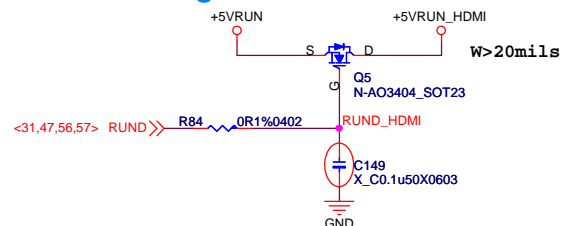
HPD\_SNK Internal PD 150kohm



## EMI Close Connector



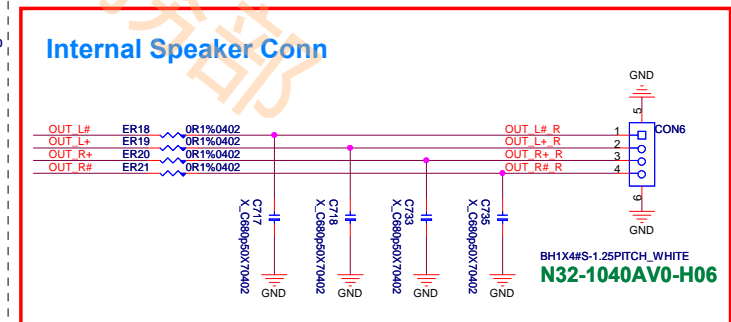
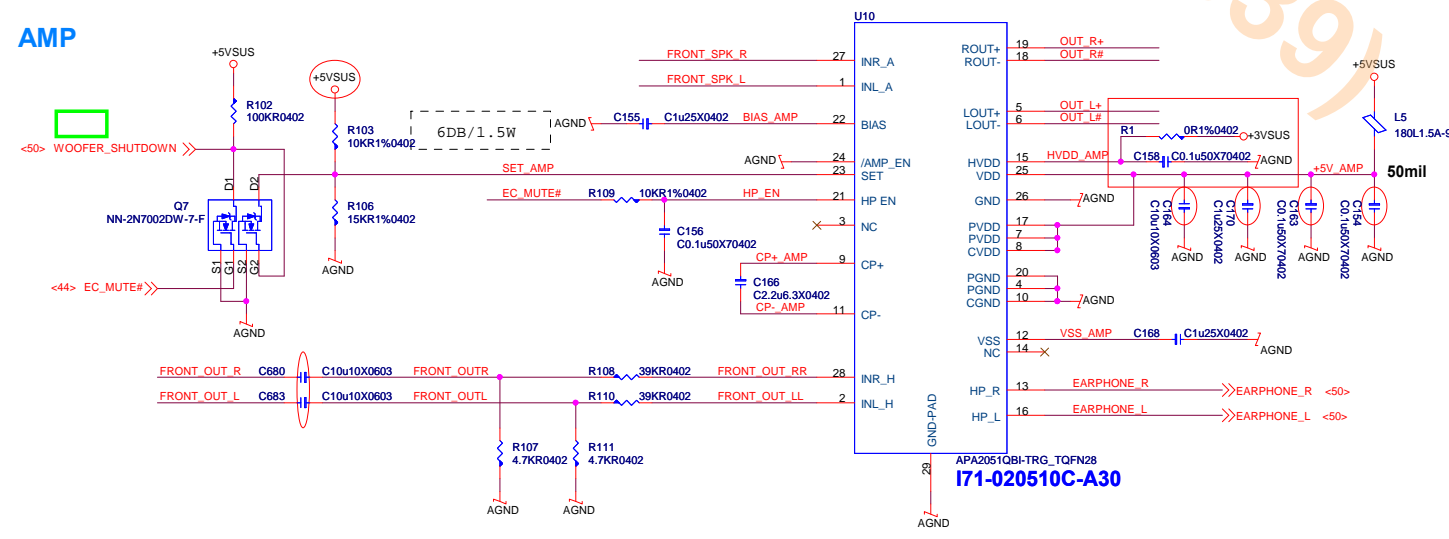
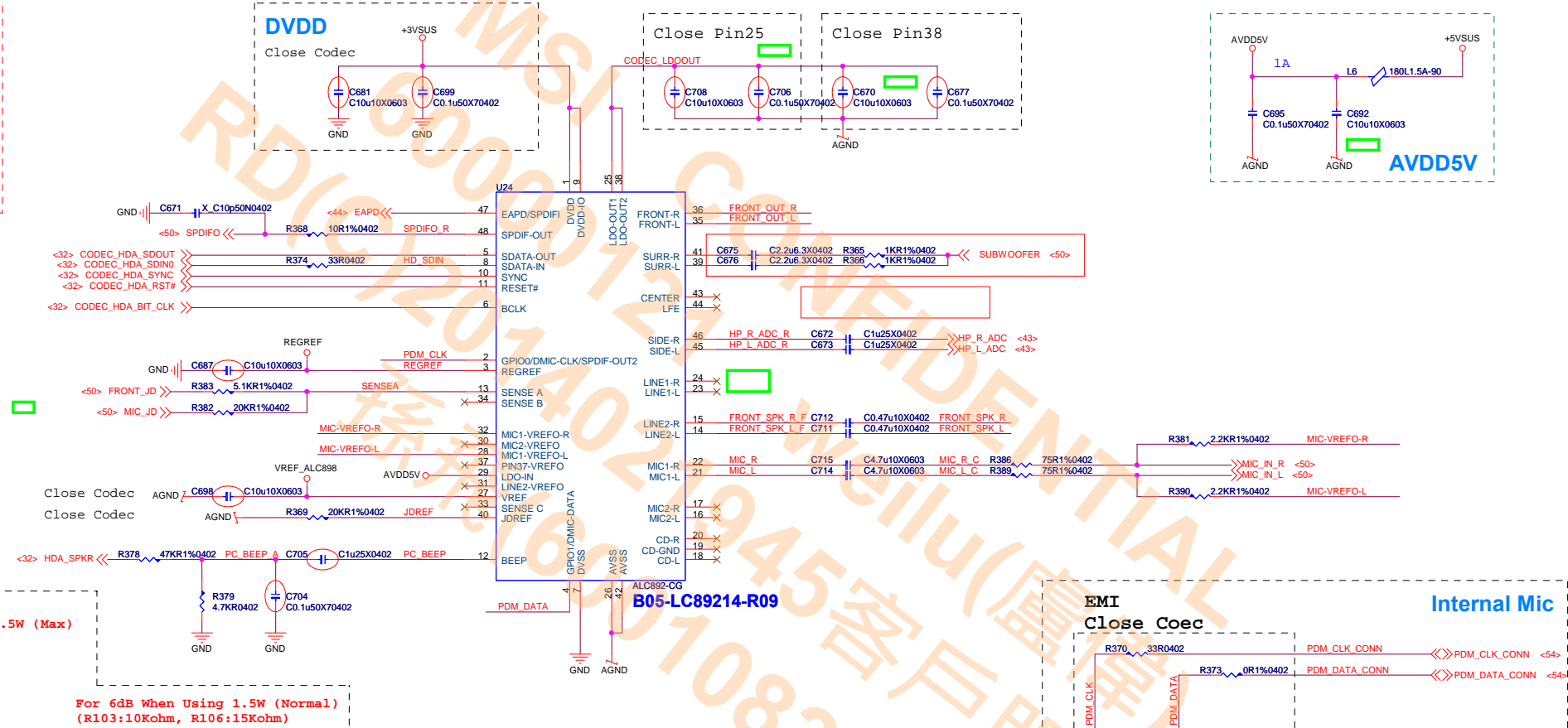
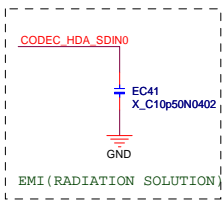
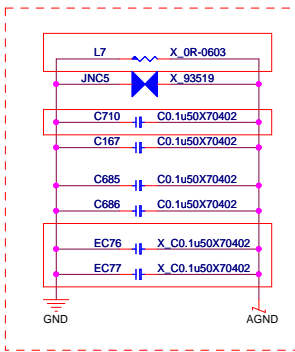
## Avoid HDMI Leakage



ADDR1 (CFG)	ADDR0 (EQ)	I2C control bus address (Internal pull down at ~150kΩ, 3.3V I/O)
0	0	0x4C / 4D (default)
0	1	0x5C / 5D
1	0	0xCC / CD
1	1	0xEC / ED

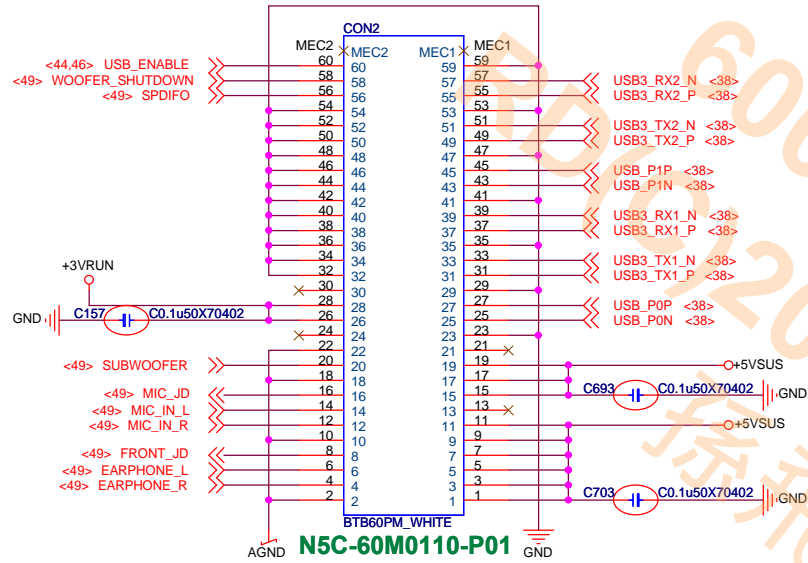


## Audio CODEC/Audio AMP

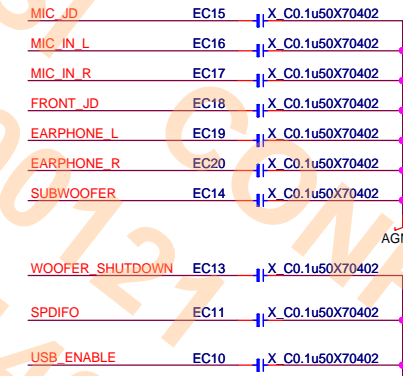


# CPU FAN/BTB CONN

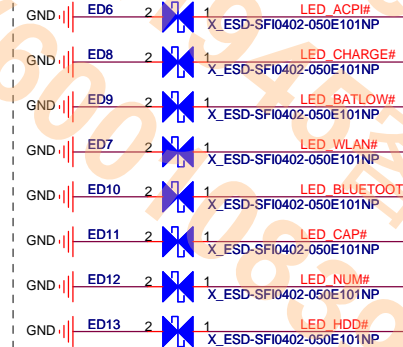
## To 16H2A(Audio CONN/USB3.0)



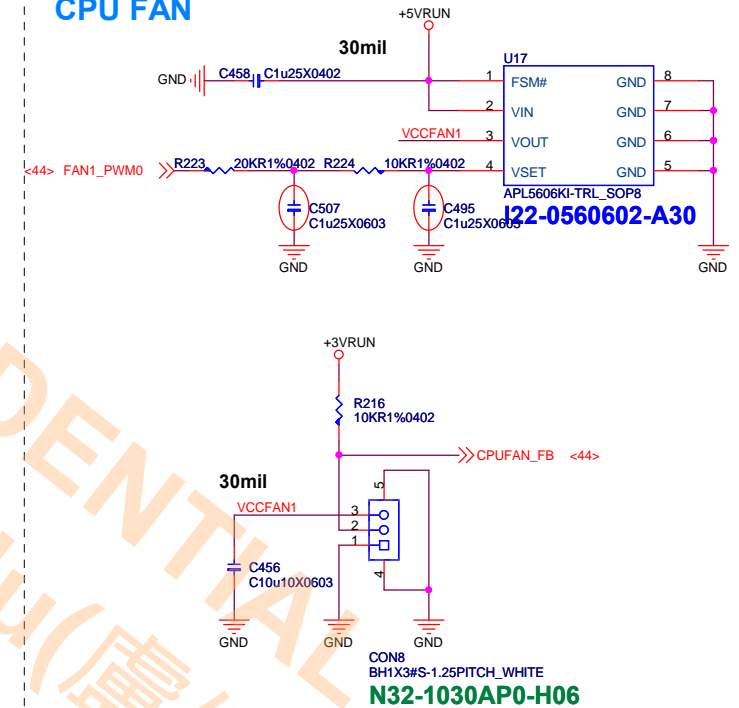
## EMI



## EMI

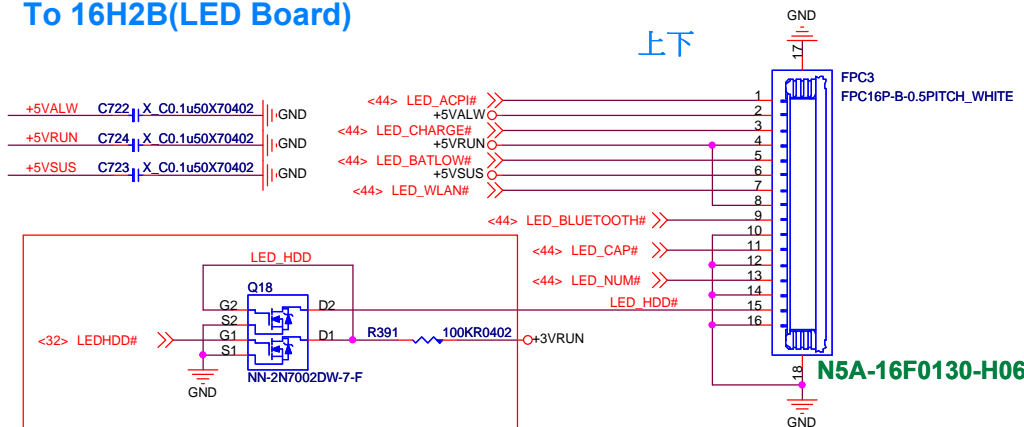


## CPU FAN



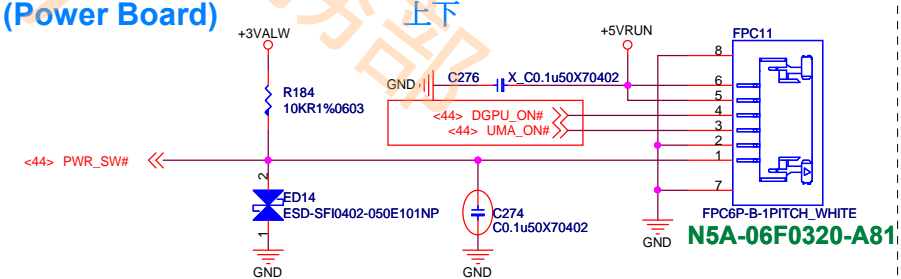
## To 16H2B(LED Board)

上下



## To 16H2C (Power Board)

上下

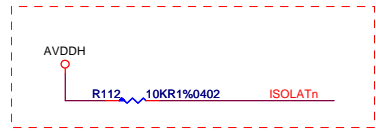


msi

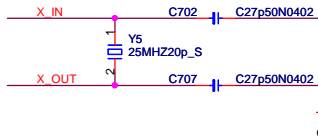
MICRO-STAR INT'L CO.,LTD.

Title		CPU FAN/BTB CONN	
Size	Document Number	MS-16H2	
Date:	Thursday, September 05, 2013	Sheet	50 of 71
		Rev	0A

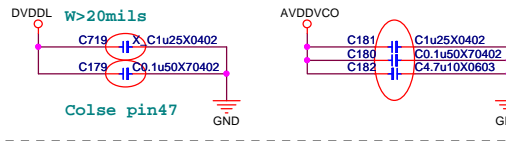
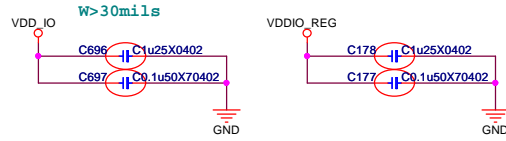
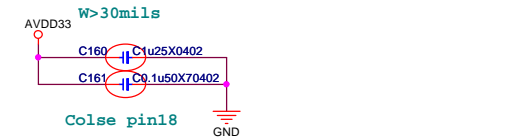
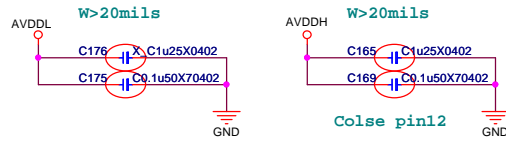
# GIGA LAN(BigFoot BFN2205B)



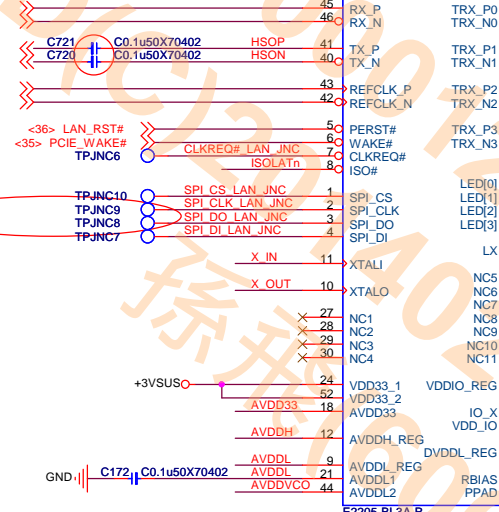
RST# spacing 20mils



## Power CAP

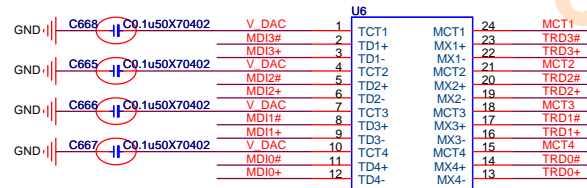


<38> PCIE\_GLAN\_TXP  
<38> PCIE\_GLAN\_TXN  
<38> PCIE\_GLAN\_RXP  
<38> PCIE\_GLAN\_RXN  
<33> CLK\_PCIE\_LAN  
<33> CLK\_PCIE\_LAN#

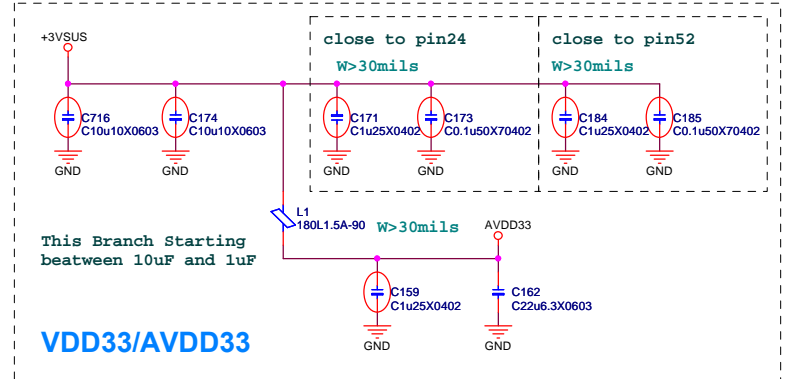
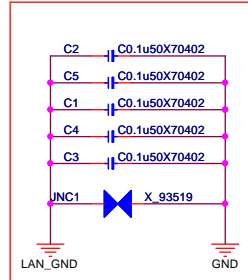
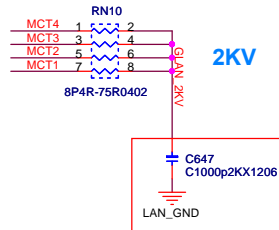


B06-E22050C-Q24

MAC 燒 CHIP  
內,有次數限制

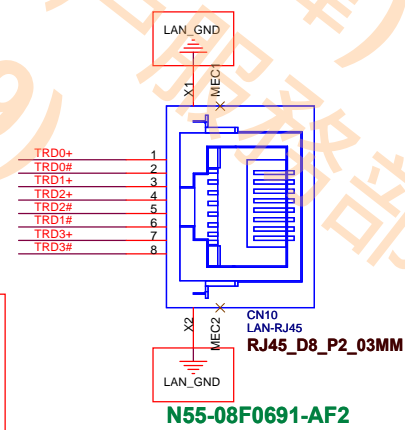
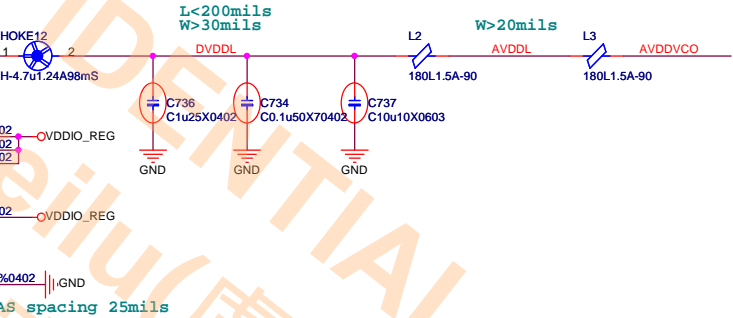


GST5009-VLF  
L05-0200150-B09

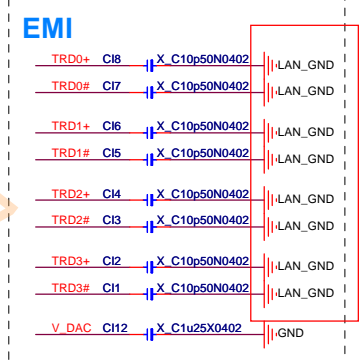


This Branch Starting  
between 10uF and 1uF

VDD33/AVDD33

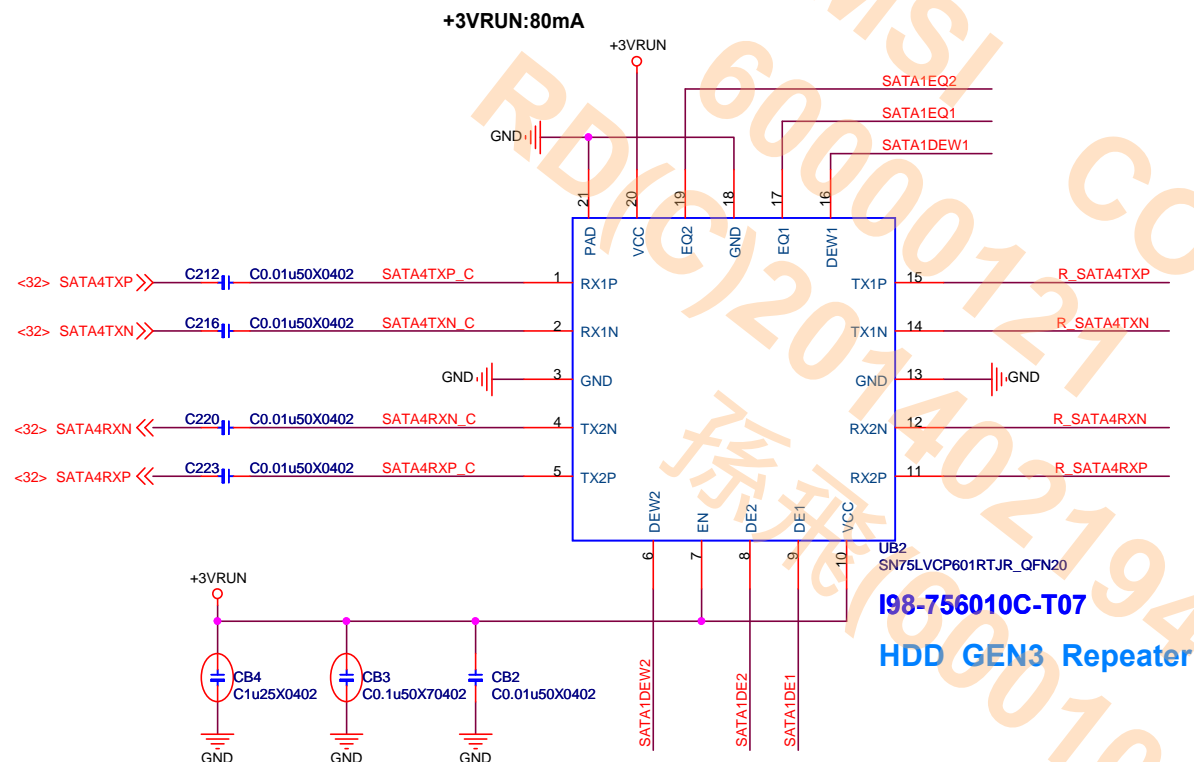


N55-08F0691-AF2

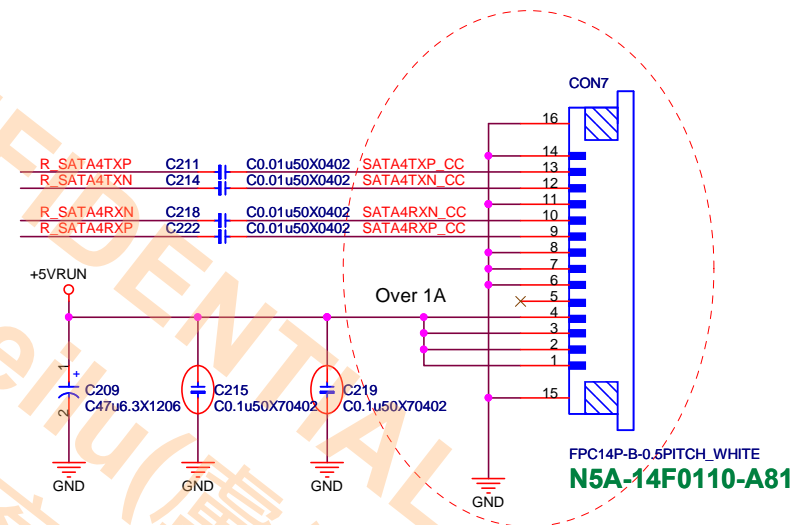


EMI

# HDD (With Repeater)



## BTB Connector



## TI SN75LVCP601RTJR HW Setting

DE1/DE2	CH1/CH2De-Emphasis dB (at 6Gbps)	EQ1/EQ2	CH1/CH2Equalization dB (at 6Gbps)
NC (default)	-4	NC (default)	0
0	0	0	7
1	-2	1	14

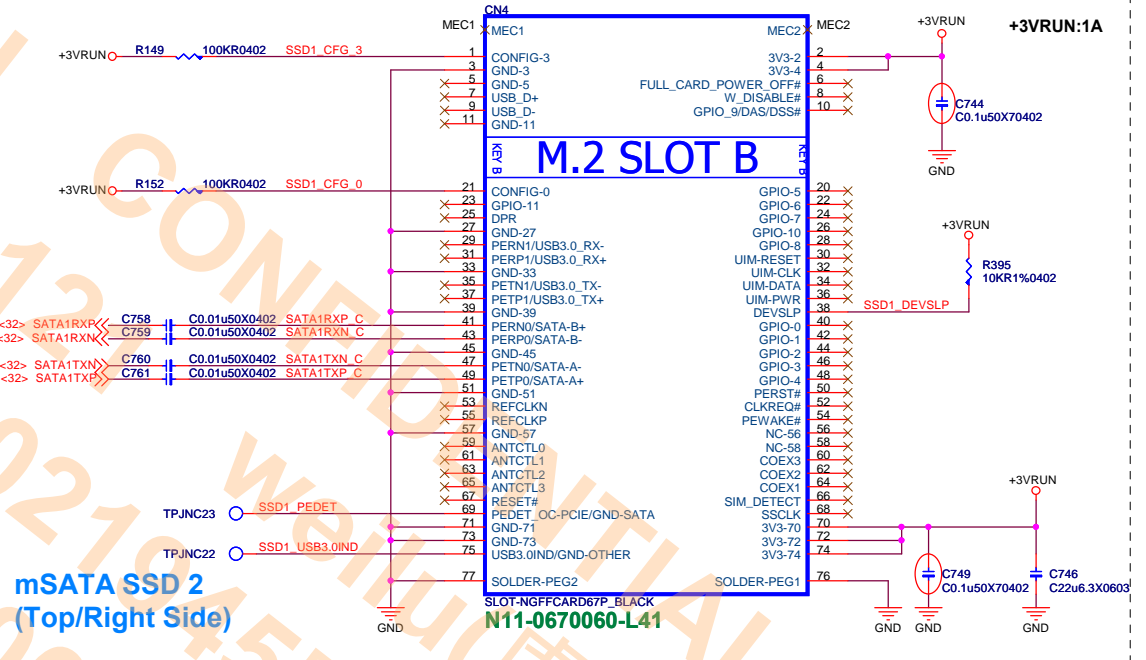
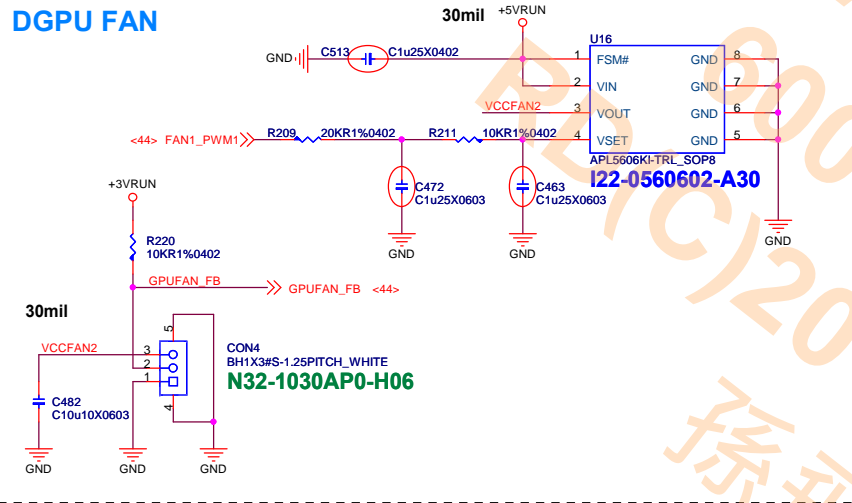
  

DEW1/DEW2	Device Function → DE Width for CH1/CH2
0	De-emphasis pulse duration, short (recommended setting when link operates at SATA 1.5/3/6 Gbps)
1 (default)	De-emphasis pulse duration, long (recommended setting when link operates at SATA 1.5/3 Gbps speed only)

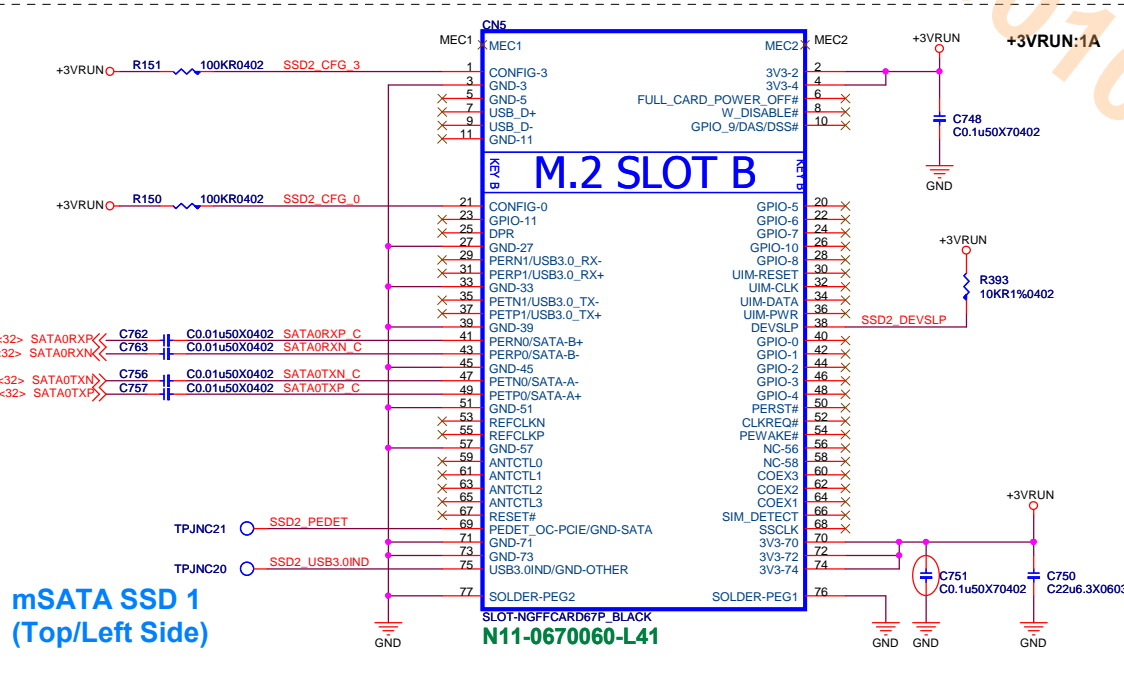


# SSD/ DGPU FAN

## DGPU FAN



## mSATA SSD 2 (Top/Right Side)

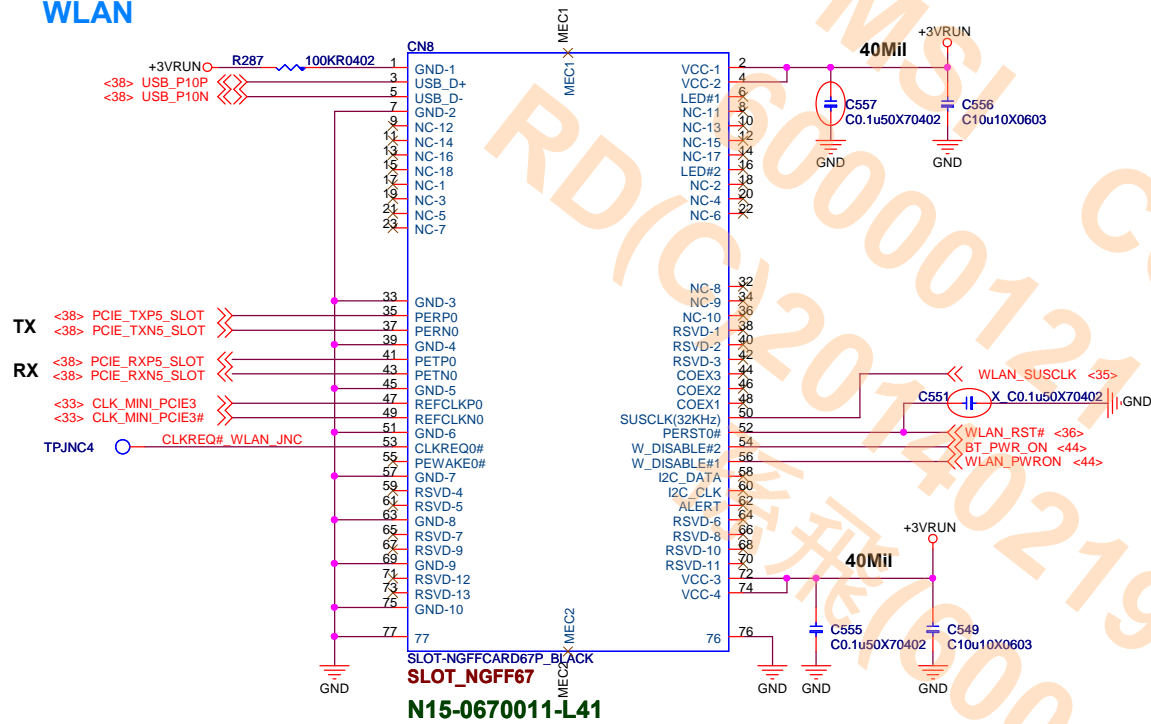


## mSATA SSD 1 (Top/Left Side)

40	NC	No Connect
41	SATA-B+/PERn0	Host receiver differential signal pair
42	NC	No Connect
43	SATA-B-/PERp0	Host receiver differential signal pair
44	NC	No Connect
45	GND	Ground
46	NC	No Connect
47	SATA-A-/PETn0	Host Transmitter differential signal pair
48	NC	No Connect
49	SATA-A+/PETp0	Host transmitter differential signal pair

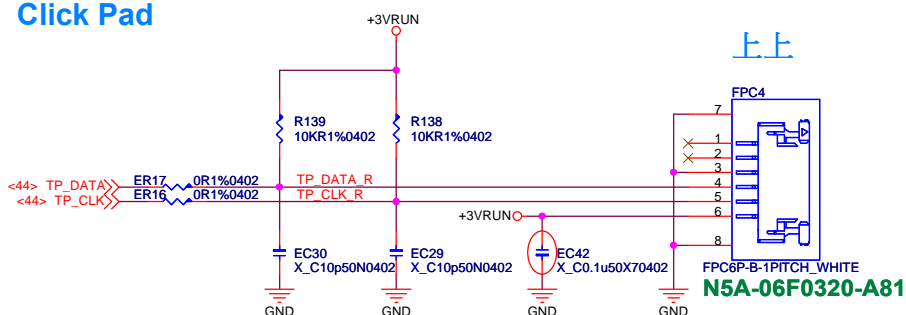


## WLAN

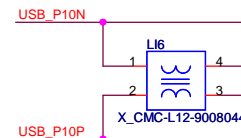


Pin 1	GND	Pin 2	3.3V
Pin 3	USB_D+	Pin 4	3.3V
Pin 5	USB_D-	Pin 6	LED1#
Pin 7	GND	Pin 8	Module Key
Pin 9	Module Key	Pin 10	Module Key
Pin 11	Module Key	Pin 12	Module Key
Pin 13	Module Key	Pin 14	Module Key
Pin 15	N/C	Pin 16	LED2#
Pin 17	N/C	Pin 18	GND
Pin 19	N/C	Pin 20	N/C
Pin 21	N/C	Pin 22	N/C
Pin 23	N/C	Pin 24	Module Key
Pin 25	Module Key	Pin 26	Module Key
Pin 27	Module Key	Pin 28	Module Key
Pin 29	Module Key	Pin 30	Module Key
Pin 31	Module Key	Pin 32	N/C
Pin 33	GND	Pin 34	N/C
Pin 35	PERP0	Pin 36	N/C
Pin 37	PERN0	Pin 38	Clink Reset (I 3.3V)
Pin 39	GND	Pin 40	N/C
Pin 41	PETP0	Pin 42	N/C
Pin 43	PETN0	Pin 44	N/C
Pin 45	GND	Pin 46	N/C
Pin 47	REFCLKP0	Pin 48	N/C
Pin 49	REFCLKN0	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 51	GND	Pin 52	PERST0#
Pin 53	CLKREQ0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 55	PEWAKE0#	Pin 56	WLAN_EN (W_DISABLE2#)
Pin 57	GND	Pin 58	N/C
Pin 59	N/C	Pin 60	N/C
Pin 61	N/C	Pin 62	N/C
Pin 63	GND	Pin 64	Resever
Pin 65	N/C	Pin 66	N/C
Pin 67	N/C	Pin 68	N/C
Pin 69	GND	Pin 70	N/C
Pin 71	N/C	Pin 72	3.3V
Pin 73	N/C	Pin 74	3.3V
Pin 75	GND		

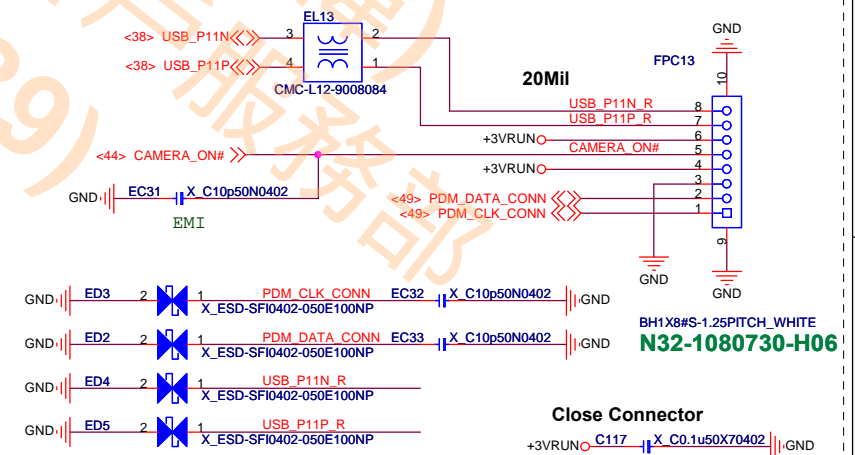
## Click Pad



## EMI



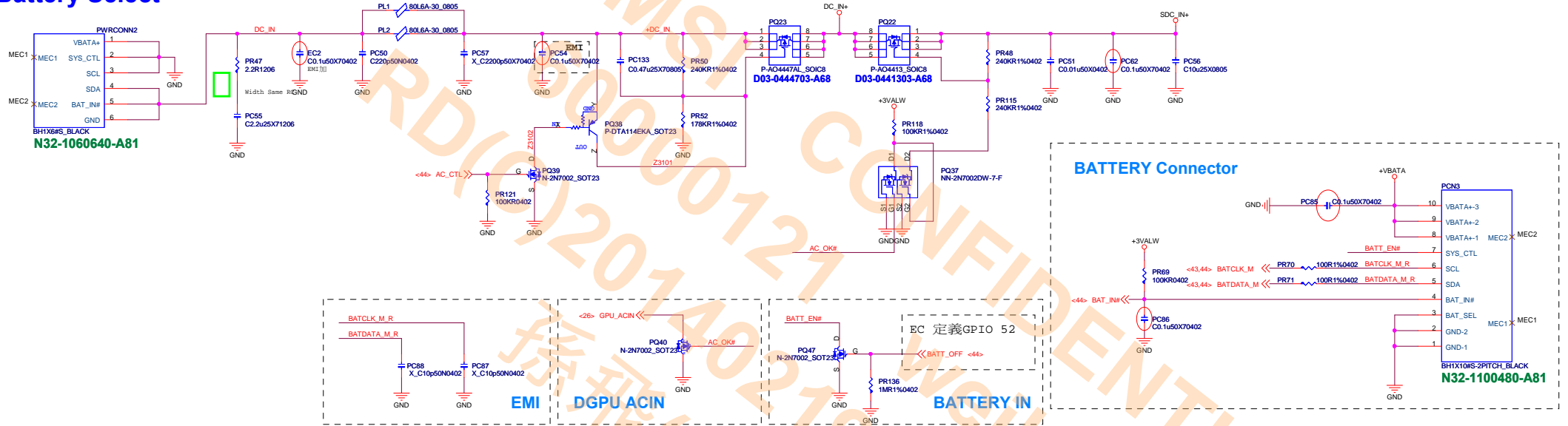
## CAMERA



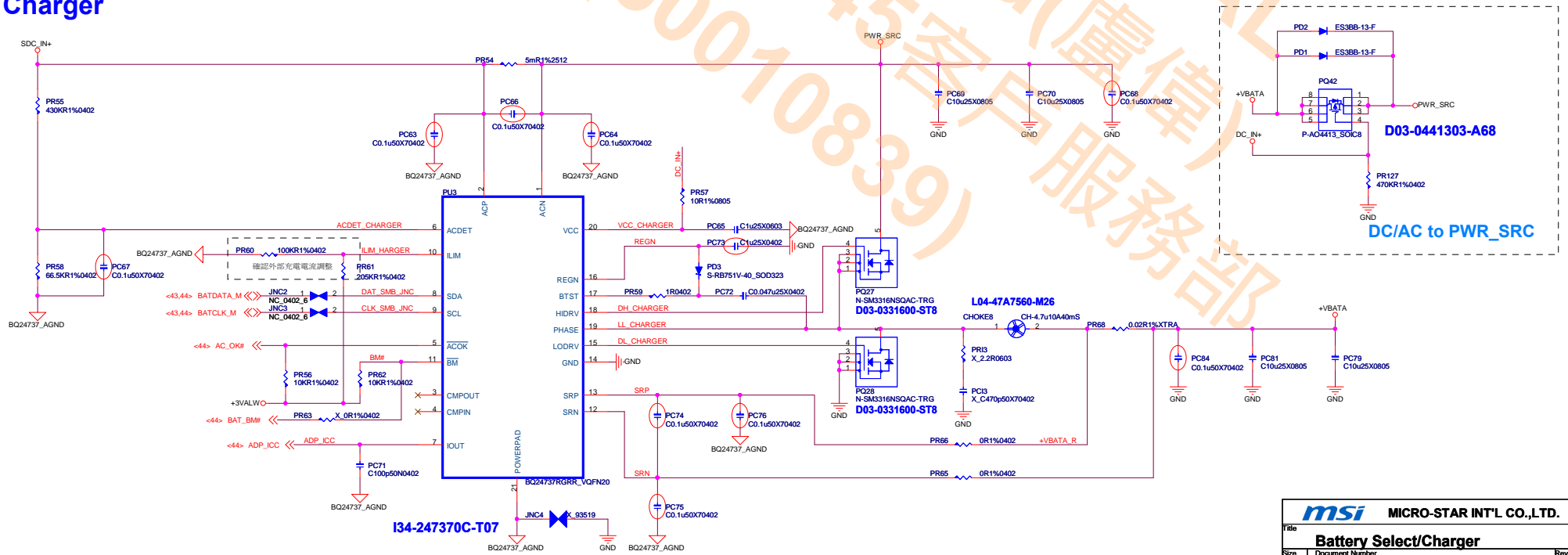


## Battery Select/Charger

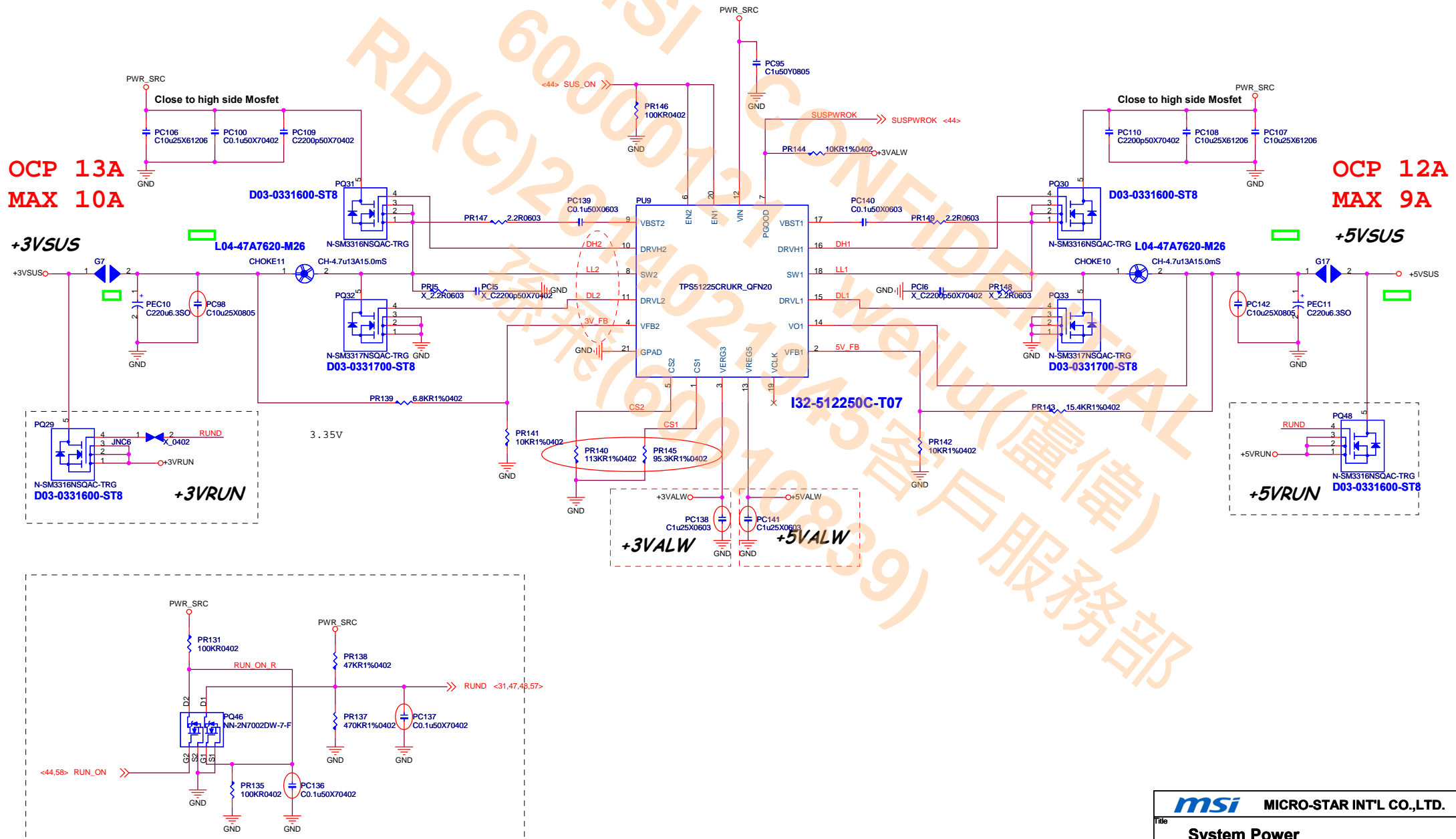
## Battery Select



## Battery Charger



## System Power



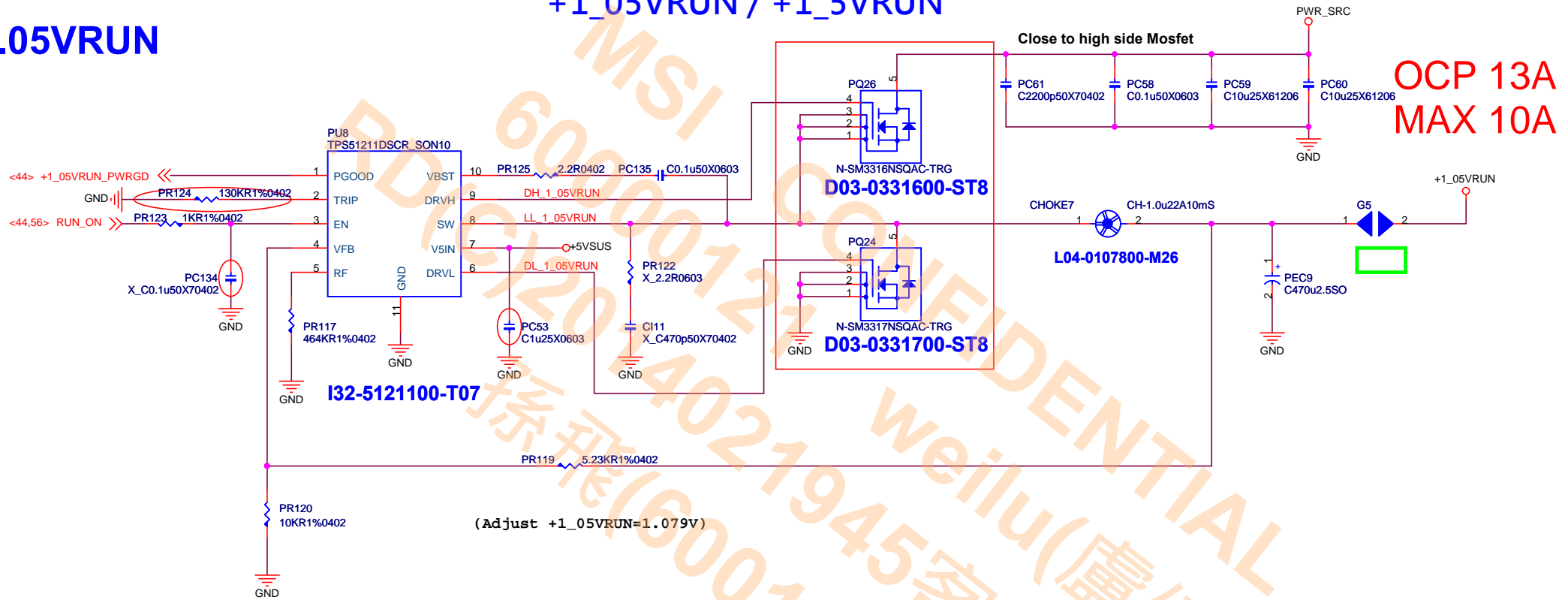
**+1.35VDIMM/+0.675VRUN**



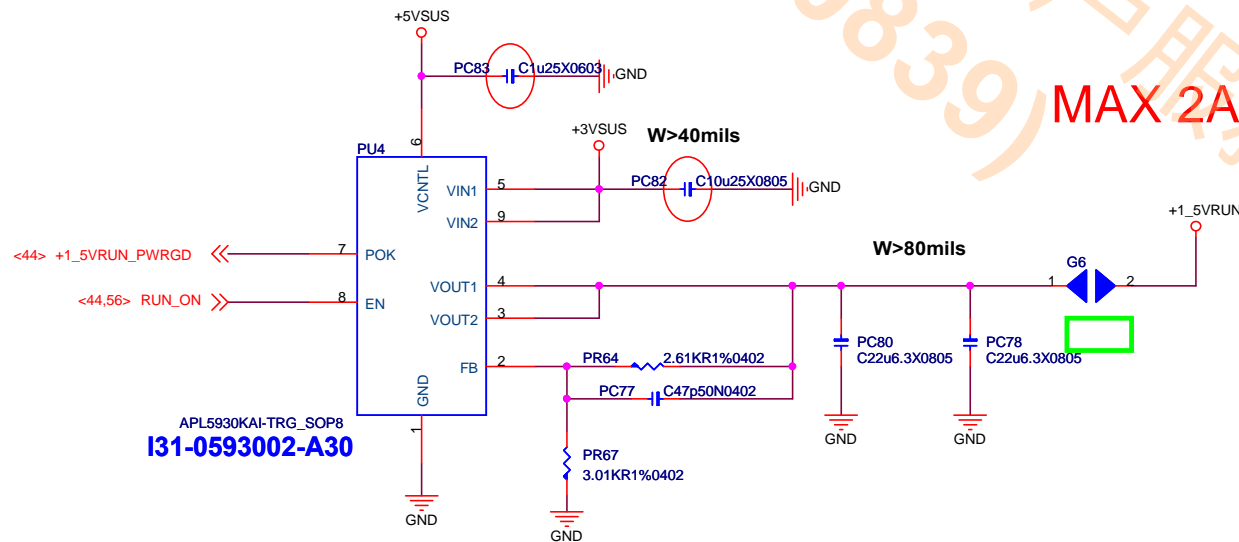
Title			
<b>+1.35VDIMM/+0.675VRUN</b>			
Size	Document Number	Rev	
	<b>MS-16H2</b>	<b>0A</b>	
Date:	Thursday, September 05, 2013	Sheet	57 of 71

# +1.05VRUN

## +1\_05VRUN / +1\_5VRUN



# +1.5VRUN



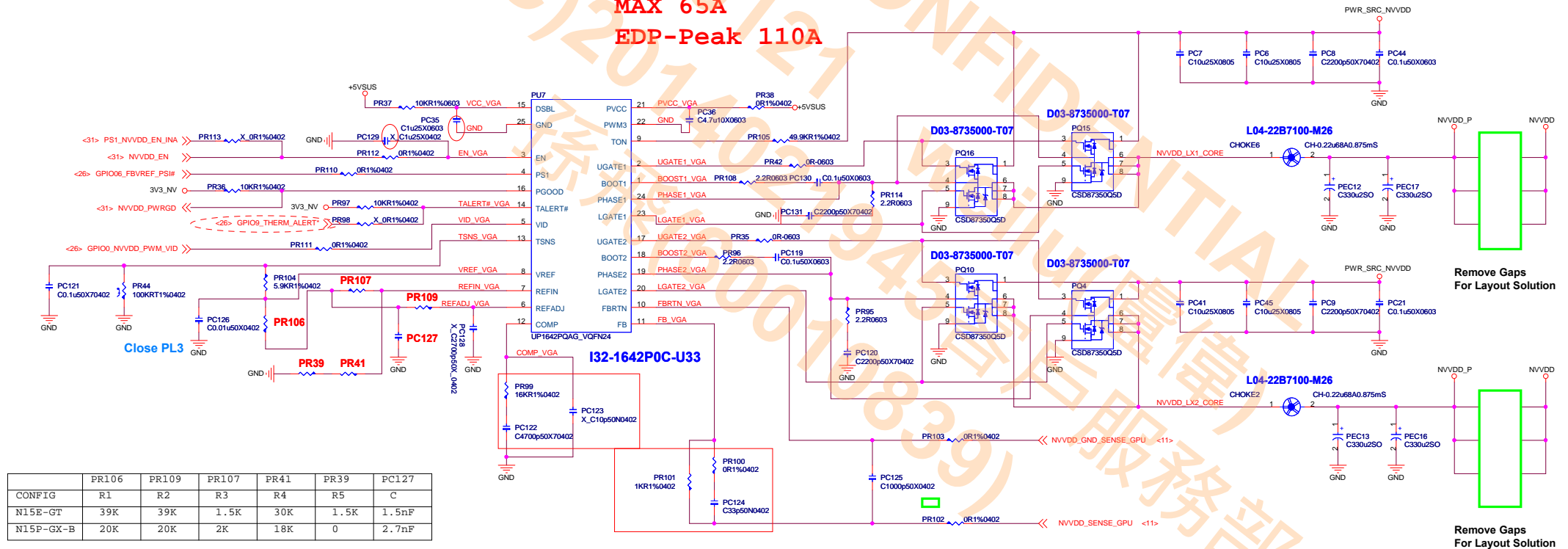


# DGPU POWER NVVDD

## DGPU POWER / UP1642PQAG

CONFIG B  
VBoot:0.9V  
Vmin:0.6V / Vmax:1.2V

MAX 65A  
EDP-Peak 110A



	PR106	PR109	PR107	PR41	PR39	PC127
CONFIG	R1	R2	R3	R4	R5	C
N15E-GT	39K	39K	1.5K	30K	1.5K	1.5nF
N15P-GX-B	20K	20K	2K	18K	0	2.7nF

### N15E-GT


DGPU_GT_R1	DGPU_GT_R2	DGPU_GT_R3	DGPU_GT_R4	DGPU_GT_R5	DGPU_GT_C1
<input type="checkbox"/> 5020	<input type="checkbox"/> 5020	<input type="checkbox"/> 5020	<input type="checkbox"/> 5020	<input type="checkbox"/> 5010	<input type="checkbox"/> 5020
R11-0393T12-W08	R11-0393T12-W08	R11-0152T12-W08	R11-0303T12-W08	R11-0152T12-W08	C11-1522812-W08
X_39KR1%0402	X_39KR1%0402	X_1.5KR1%0402	X_30KR1%0402	X_1.5KR1%0402	X_C1500p50X0402

### N15P-GX-B

DGPU_GX_R1	DGPU_GX_R2	DGPU_GX_R3	DGPU_GX_R4	DGPU_GX_R5	DGPU_GX_C1
<input type="checkbox"/> 5020	<input type="checkbox"/> 5020	<input type="checkbox"/> 5020	<input type="checkbox"/> 5020	<input type="checkbox"/> 5010	<input type="checkbox"/> 5020
R11-0203T12-W08	R11-0203T12-W08	R11-0202T12-W08	R11-0183T12-W08	R11-0000T12-Y01	C11-2722812-W08
X_20KR1%0402	X_20KR1%0402	X_2KR1%0402	X_18KR1%0402	X_0R1%0402	X_C2700p50X_0402



## CPU Power (+VCC\_CORE)

		<b>MICRO-STAR INT'L CO.,LTD.</b>	
<b>Title</b>			
<b>CPU Power (ISL95812HRZ)</b>			
<b>Size</b>	<b>Document Number</b>		<b>Rev</b>
	<b>MS-16H2</b>		<b>0A</b>
<b>Date:</b>	<b>Thursday, September 05, 2013</b>	<b>Sheet</b>	<b>61 of 71</b>

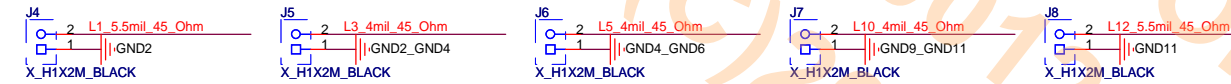
# EMI/ Impedance

## Impedance Connector No PN

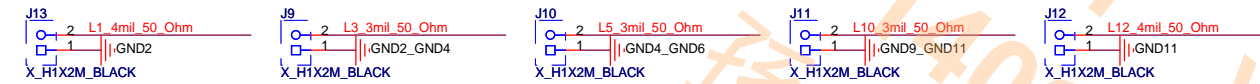
40 ohm



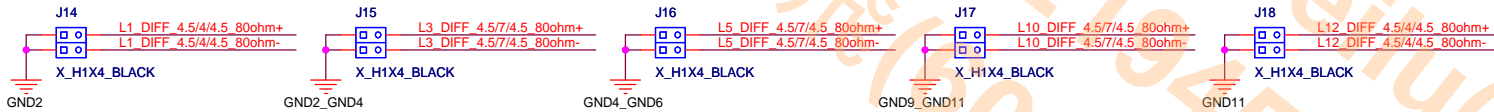
45 ohm



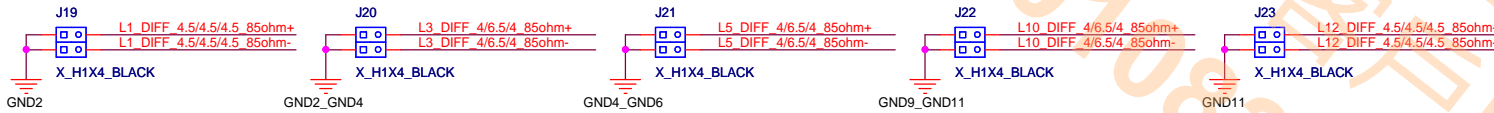
50 ohm



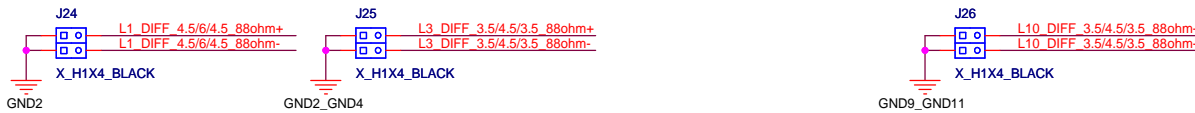
80 ohm



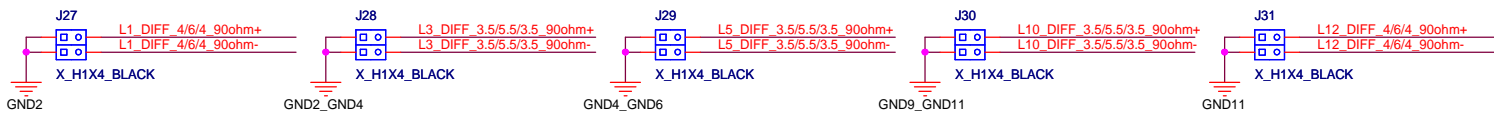
85 ohm



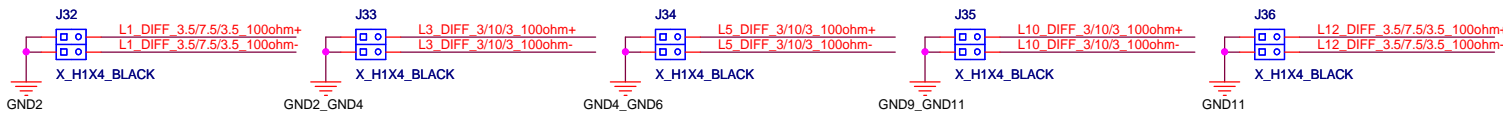
88 ohm



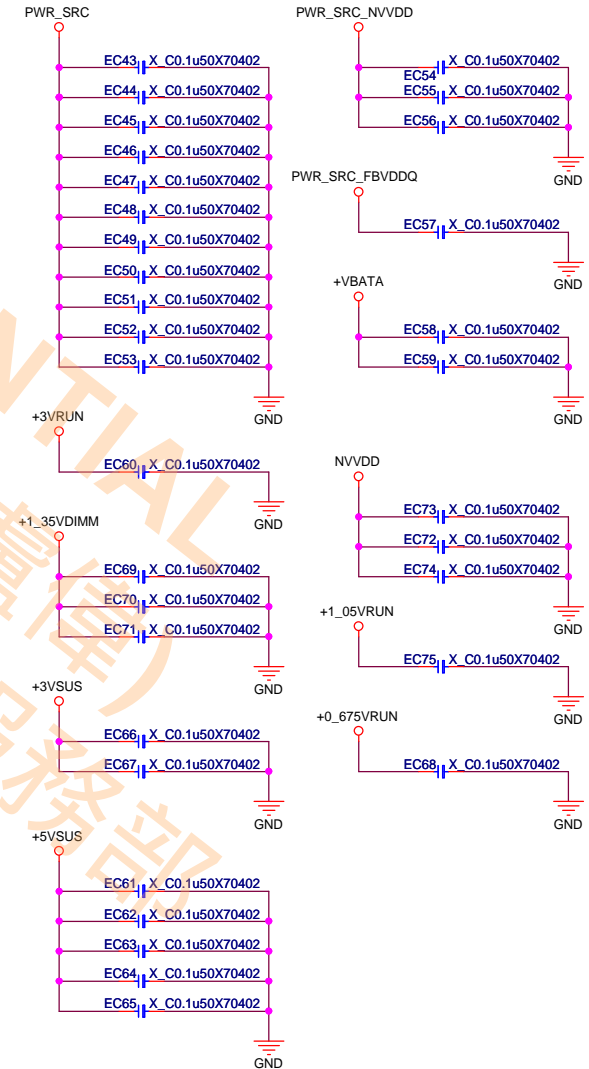
90 ohm



100 ohm



## EMI



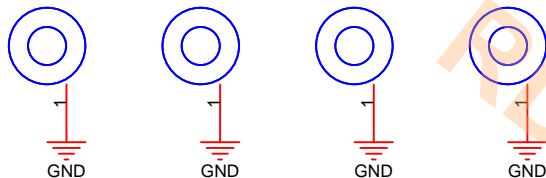
msi

MICRO-STAR INT'L CO.,LTD.

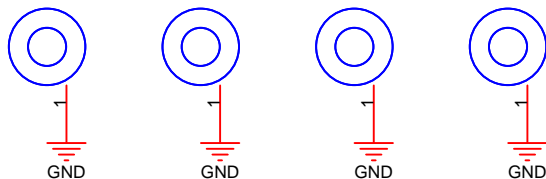
Title			EMI/ Impedance
Size			Document Number
			MS-16H2
Date:			Thursday, September 05, 2013
Sheet			62 of 71
Rev			0A

## CPU/GPU Holes

MCPU4 H\_R276D169\_PB  
MCPU2 H\_R276D169\_PB  
MCPU3 H\_R276D169\_PB  
MCPU1 H\_R276D169\_PB

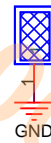


MGPU2 H\_R276D169\_PB  
MGPU4 H\_R276D169\_PB  
MGPU1 H\_R276D169\_PB  
MGPU3 H\_R276D169\_PB



## EMI

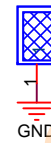
SPRING1  
HS-MS1011



E23-1011040-CA7

ATE\_C006\_106

SPRING2  
HS-MS1011



E23-1011040-CA7

ATE\_C006\_106

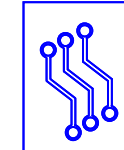
SPRING3  
HS-MS1011



E23-1011040-CA7

ATE\_C006\_106

PCB1

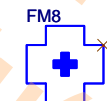
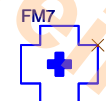
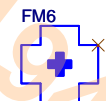
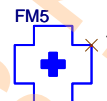


P30-16H210A-H73

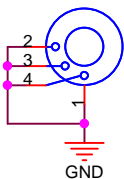
**P30-16H210A-H73**

Hannstar: P30-16H210A-H73

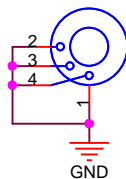
TRIPOD: P30-16H210A-T53



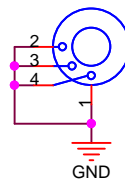
M2  
X\_H\_R197D118\_PT\_V3  
H\_R197D118\_PT\_V3



M1  
X\_H\_R197D118\_PT\_V3  
H\_R197D118\_PT\_V3

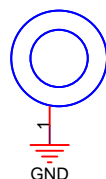


M7  
X\_H\_R197D118\_PT\_V3  
H\_R197D118\_PT\_V3



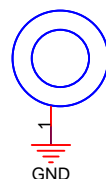
## Fan Hole

MH1  
H\_R197D91  
X\_ME\_ SCREW HOLE

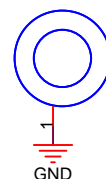


## SSD Stand off

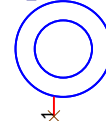
MH3  
H\_R220D146\_PTB  
E2B-16H2020



MH2  
H\_R220D146\_PTB  
E2B-16H2020



MH4  
NPTH157  
X\_NPTH157



UME1



X\_HDMI ROYALTY

**Y01-RHDMI03-000**

For MP

UME2



X BIOS\_LABEL

**G51-LA01678-A09**

**msi**

**MICRO-STAR INT'L CO.,LTD.**

Title

**Screw/ME**

Size

Document Number

**MS-16H2**

Rev

**0A**

Date: Monday, September 09, 2013

Sheet 63 of 71